QIQY5

Whisky3.0 (Y490)

LA-8691P Rev0.2 Schematic

Intel IVY Bridge Processor with DDRIII + Panther Point PCH
nVIDIA N13P GT1-A2 + 2nd VGA N13P GT1-A2

2012-02-05 Rev0.2

Security Classification	Compal Secret Data		
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Title: *Cover Page*		
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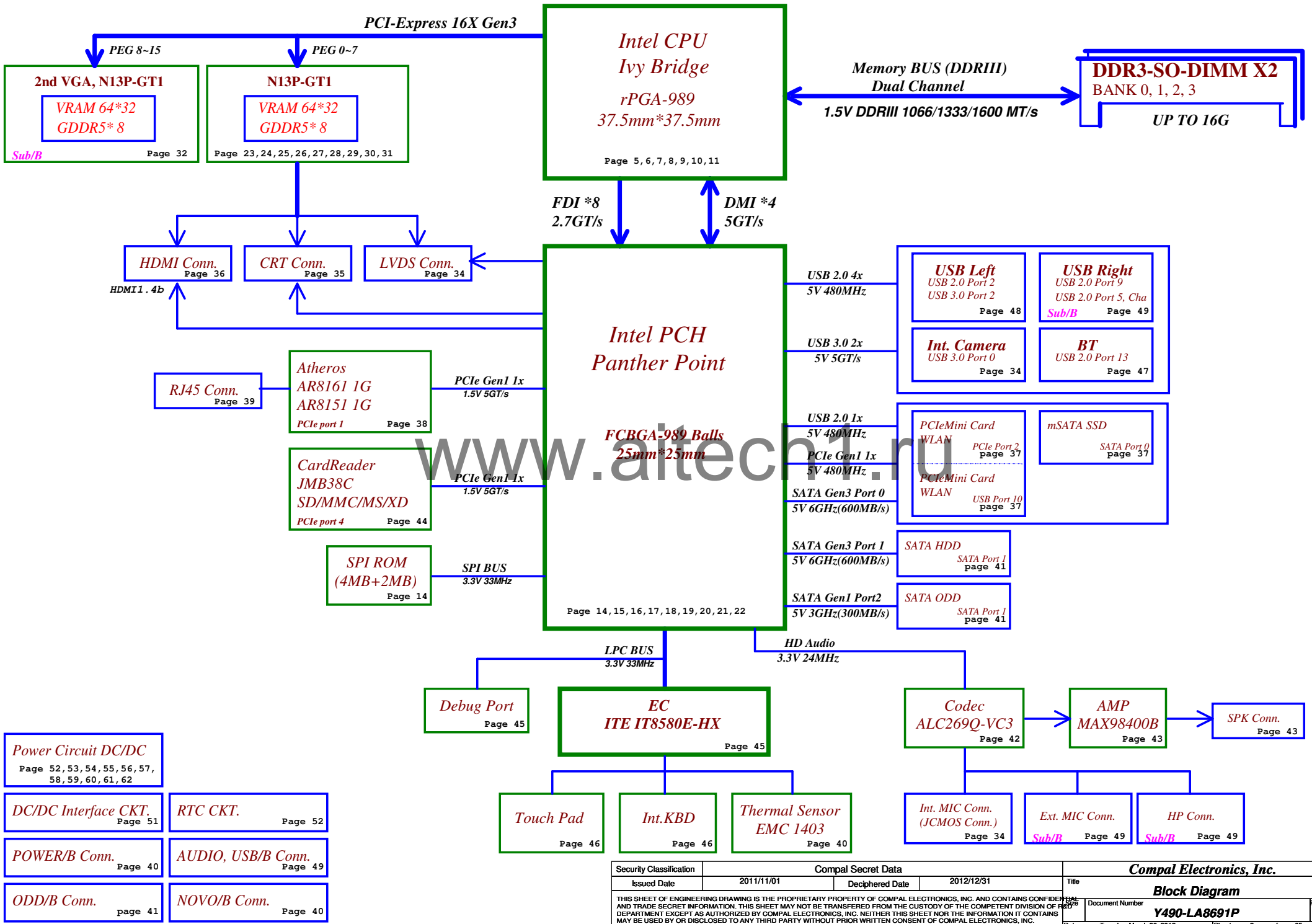

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Title: Block Diagram

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Voltage Rails (O --> Means ON , X --> Means OFF)

Power Plane / State	B+	+3VALW +5VALW	+1.5V	+5VS +3VS +1.5VS +VCCSA +V1.5S_VCCP +CPU_CORE +VGA_CORE +GFX_CORE +1.8VS +1.05VS +0.75VS +3.3VS_VGA +1.5VS_VGA +1.05VS_VGA
S0	O	O	O	O
S3	O	O	O	X
S5 S4/AC Only	O	O	X	X
S5 S4 Battery only	O	X	X	X
S5 S4 AC & Battery don't exist	X	X	X	X

STATE / SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

USB Port Table

USB 2.0	USB 3.0	Port	4 External USB Port
EHCI1	XHCI 1	0	Camera
	2	1	
	3	2	USB Port (Left Side)
	4	3	
		4	
		5	USB Port (Right Side)
		6	
		7	
EHCI2		8	
		9	USB Port (Right Side)
		10	Mini Card(WLAN)
		11	
		12	
		13	Blue Tooth

BOM Structure Table

BOM Structure	BTO Item
HDMI@	HDMI part
CHG@	USB charger part
NOCHG@	No USB charger part
CMOS@	CMOS Camera part
8161@	AR8161 LAN part
8151@	AR8151 LAN part
8161S@	AR8161 LAN surge part
8151S@	AR8151 LAN surge part
SURGE@	AR8151&8161 LAN surge part
61@	X76 P/N for AR8161
51@	X76 P/N for AR8151
X76@	X76 Level part for VRAM
GC6@	NV CG6 support part
NOGC6@	NV no CG6 support part
AOAC@	AOAC support part
KBL@	K/B Light part
ME@	ME part
OPT@	For optimus function part
SLI@	For SLI function part
DS3@	Deep S3 support part
S3@	For S3 function part
GT@	NV chip part
@	Unpop

SMBUS Control Table

	SOURCE	Main VGA	2nd VGA	BATT	IT8580E	SODIMM	WLAN WiMAX	Thermal Sensor	PCH	TP Module
EC_SMB_CK1 EC_SMB_DA1	IT8580E +3VALW	X	X	V +3VALW	X	X	X	X	X	X
EC_SMB_CK2 EC_SMB_DA2	IT8580E +3VS	V +3VS	V +3VS	X	X	X	X	V +3VS	V +3V_PCH	X
SMB_CLK_S3 SMB_DATA_S3	PCH +3VS	X	X	X	X	V +3VS	V +3VS	X	V +3V_PCH	V +3VS

PCIE PORT LIST

Port	Device
1	LAN
2	WLAN
3	
4	Card Reader
5	
6	
7	
8	

EC SM Bus1 address

Device	Address
Smart Battery	0001 011X b

EC SM Bus2 address

Device	Address
Thermal Sensor EMC1403-2	1001_101xb
Master VGA	0x9E
Slave VGA	0x9C

PCH SM Bus address

Device	Address
DDR DIMM0	1001 000Xb
DDR DIMM2	1001 010Xb

ZZZ1

DA80000T10J

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Title: *Notes List*

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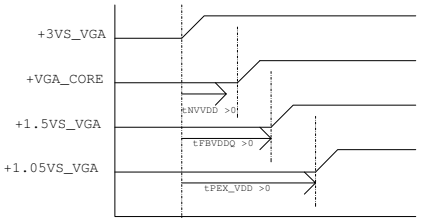
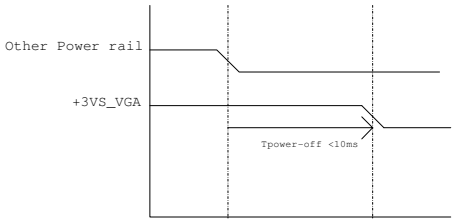
Hot plug detect for IFP link E

VGA and GDDR5 Voltage Rails (N13Px GPIO)

GPIO	I/O	ACTIVE	Function Description
GPIO0	OUT	-	GPU VID4
GPIO1	OUT	-	GPU VID3
GPIO2	OUT	_	VGA_BL_PWM
GPIO3	OUT	_	VGA_ENVDD
GPIO4	OUT	_	VGA_ENBKL
GPIO5	OUT	-	GPU VID1
GPIO6	OUT	-	GPU VID2
GPIO7	OUT	_	DPRSLPVR_VGA
GPIO8	I/O	-	Thermal Catastrophic Over Temperature
GPIO9	OUT	-	GPIO9
GPIO10	OUT	-	Memory VREF Control
GPIO11	OUT	-	GPU VID0
GPIO12	IN		AC Power Detect Input (10K pull High)
GPIO13	OUT	-	GPU VID5
GPIO14	OUT	_	FB_CLAMP_TOGGLE_REQ#
GPIO15	IN	N/A	(100K pull low)
GPIO16	OUT	_	FRMLCK#
GPIO17	IN	N/A	
GPIO18	IN	-	dGPU_HDMI_HPD
GPIO19	IN	_	HPD_IRQ



1. all power rail ramp up time should be larger than 40us



1.all GPU power rails should be turned off within 10ms
2. Optimus system VDD33 avoids drop down earlier than NVDD and FBVDDQ

Performance Mode P0 TDP at Tj = 102 C* (GDDR5)

Products	GPU (4) (W)	Mem (1,5) (W)	NVCLK /MCLK (MHz)	NVVDD (V)	NVVDD (A)	NVVDD (W)	FBVDD (1.35V) (A)	FBVDD (1.35V) (W)	FBVDDQ (GPU+Mem) (1.35V) (A)	FBVDDQ (GPU+Mem) (1.35V) (W)	PCI Express (1.05V) (6) (mA)	PCI Express (1.05V) (6) (W)	I/O and PLLVDD (1.8V) (mA)	I/O and PLLVDD (1.8V) (W)	I/O and PLLVDD (1.05V) (mA)	I/O and PLLVDD (1.05V) (W)	Other (3.3V) (mA)	Other (3.3V) (W)
N13X 128bit 1GB GDDR5	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD

Physical Strapping pin	Power Rail	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SCLK	+3VS_VGA	PCI_DEVID[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLL_EN_TERM
ROM_SI	+3VS_VGA	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SO	+3VS_VGA	FB[1]	FB[0]	SMB_ALT_ADDR	VGA_DEVICE
STRAP0	+3VS_VGA	USER[3]	USER[2]	USER[1]	USER[0]
STRAP1	+3VS_VGA	3GIO_PAD_CFG_ADR[3]	3GIO_PAD_CFG_ADR[2]	3GIO_PAD_CFG_ADR[1]	3GIO_PAD_CFG_ADR[0]
STRAP2	+3VS_VGA	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
STRAP3	+3VS_VGA	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
STRAP4	+3VS_VGA	RESERVED	PCIE_SPEED_ CHANGE_GEN3	PCIE_MAX_SPEED	DP_PLL_VDD33V

	Device ID
N13P-GT (28nm)	0x0FDB

	setting	I2C Slave addrees ID
SMB_ALT_ADDR (ROM_SO Bit 1)	0	0x9E
	1	0x9C

GPU	ROM_SO	ROM_SCLK	STRAP0	STRAP1	STRAP2	STRAP3	STRAP4	
N13P-GT1 28nm	PU 10K	PU 25K	PU 45K	PD 35K	PD 10K	PU 5K	PD 10K	Master
	PU 20K	PU 25K	PU 45K	PD 35K	PD 10K	PD 5K	PD 10K	Slave

GPU		N13P-GT		
FB Memory (GDDR5)		ROM_SI		
Samsung 2500MHz	K4G10325FG-HC04			
	32Mx32	PD 45K		
Hynix 2500MHz	H5GQ1H24BFR-T2C			
	32Mx32	PD 35K		
Samsung 2500MHz	K4G20325FD-FC04			
	64Mx32	PD 30K		
Hynix 2500MHz	H5GQ2H24MFR-T2C			
	64Mx32	PD 25K		

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Title: VGA Notes List

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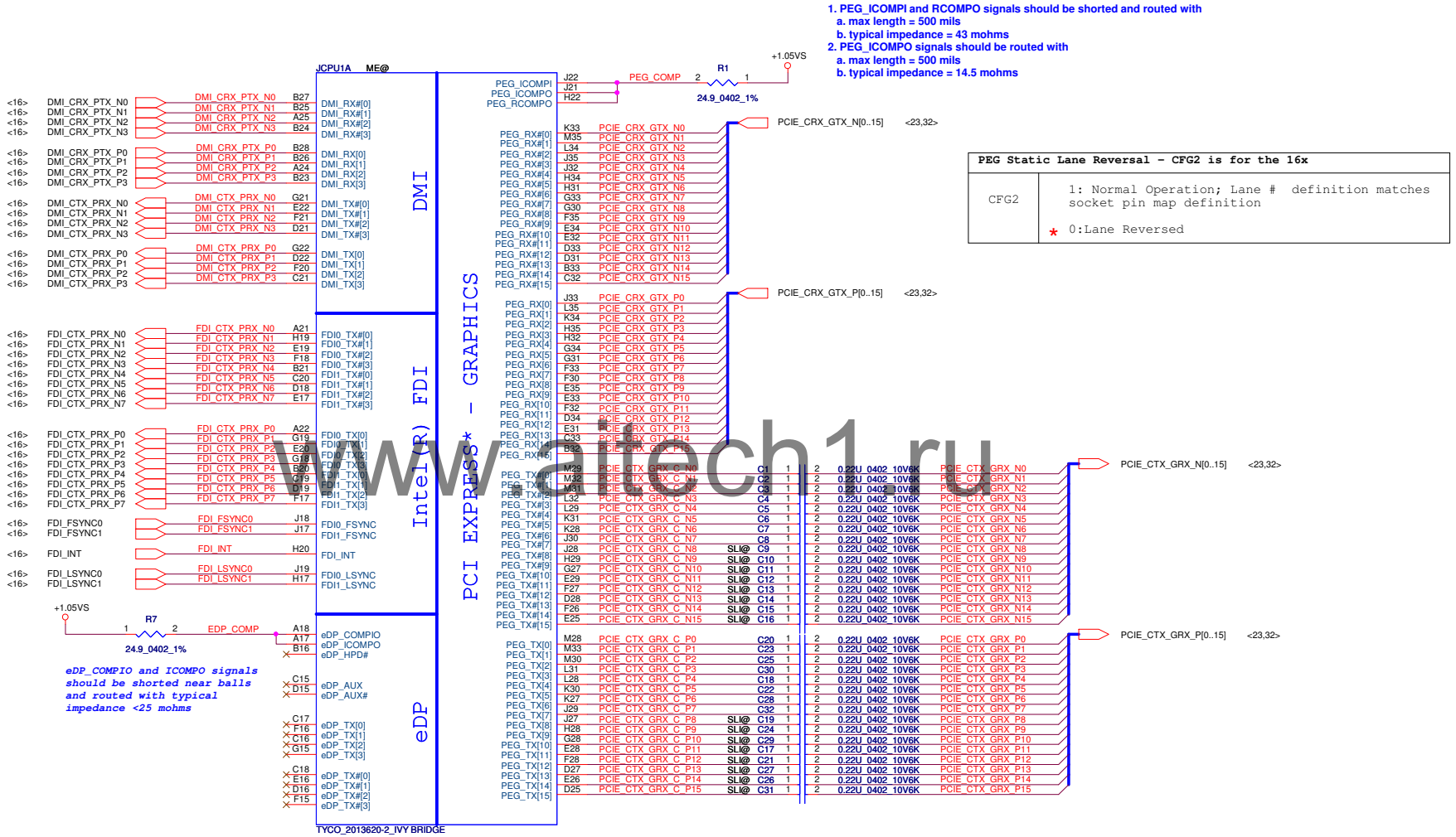

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Title: PROCESSOR(1/7) DMI,FDI,PEG

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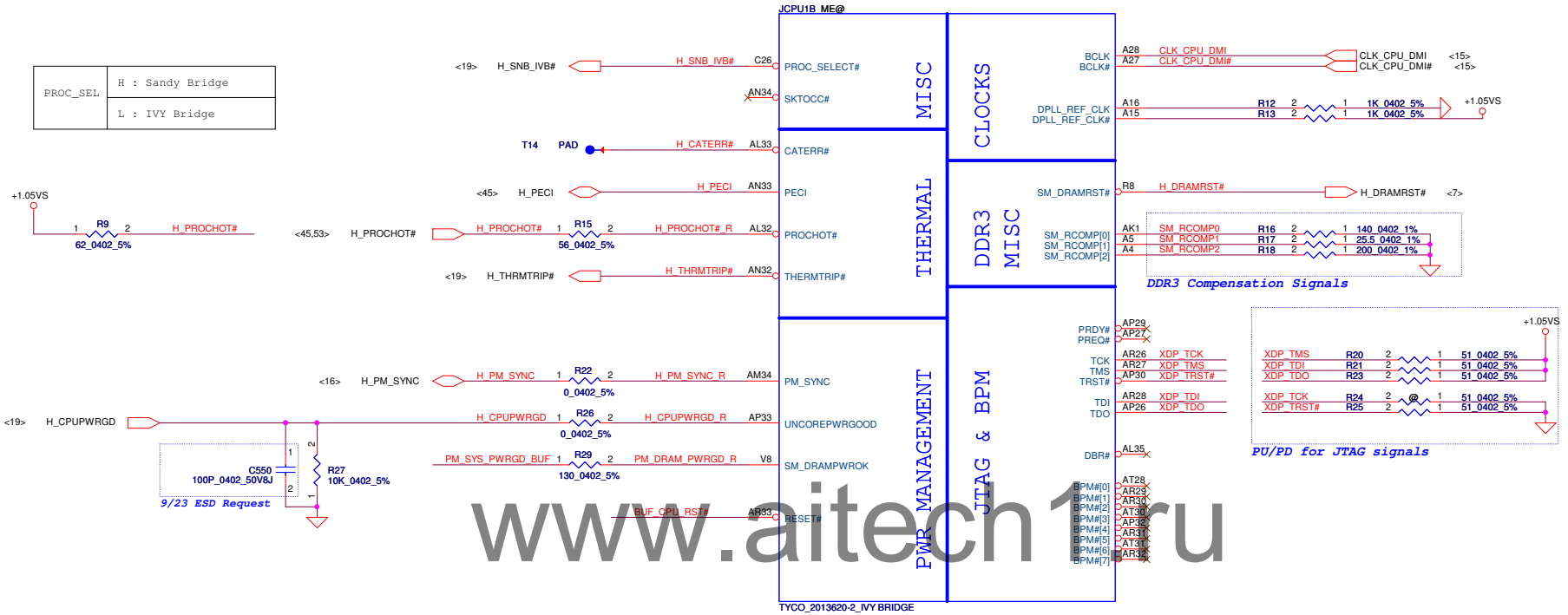
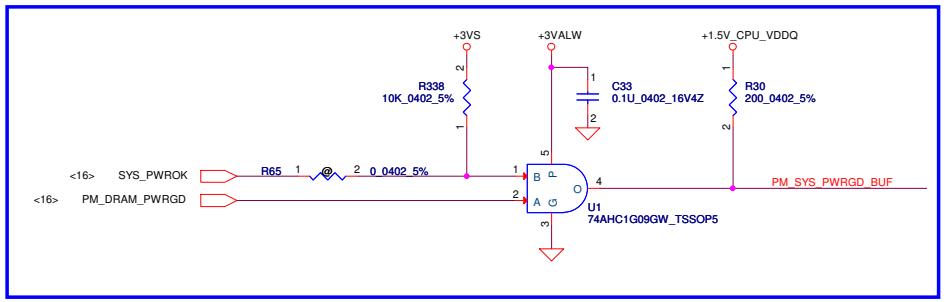
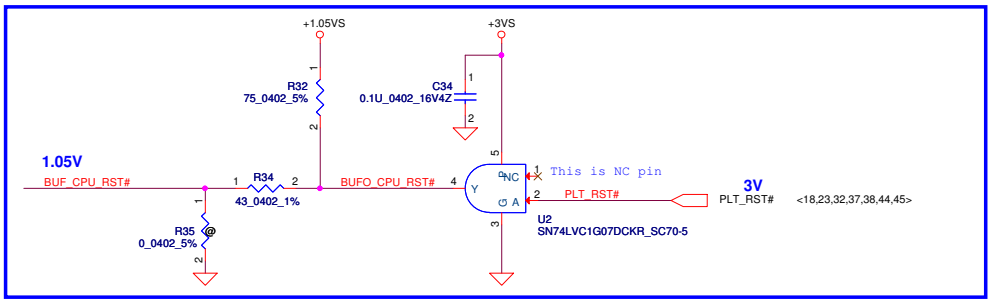




Buffered Reset to CPU



Security Classification	Compal Secret Data		
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Title: PROCESSOR(2/7) PM,XDP,CLK

Size: Custom | Document Number: Y490-LA8691P | Rev: 0.2

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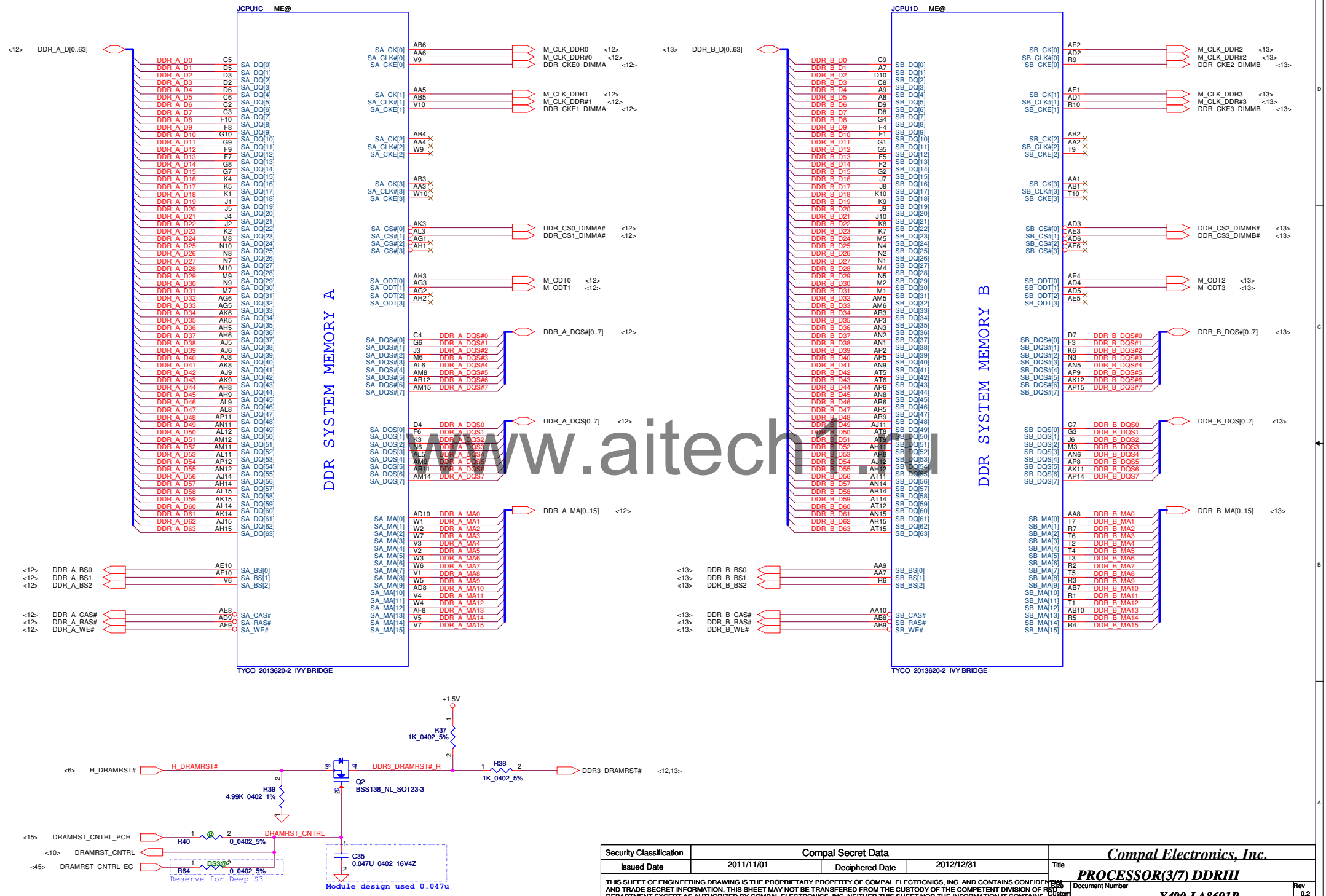

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Title: PROCESSOR(3/7) DDRIII

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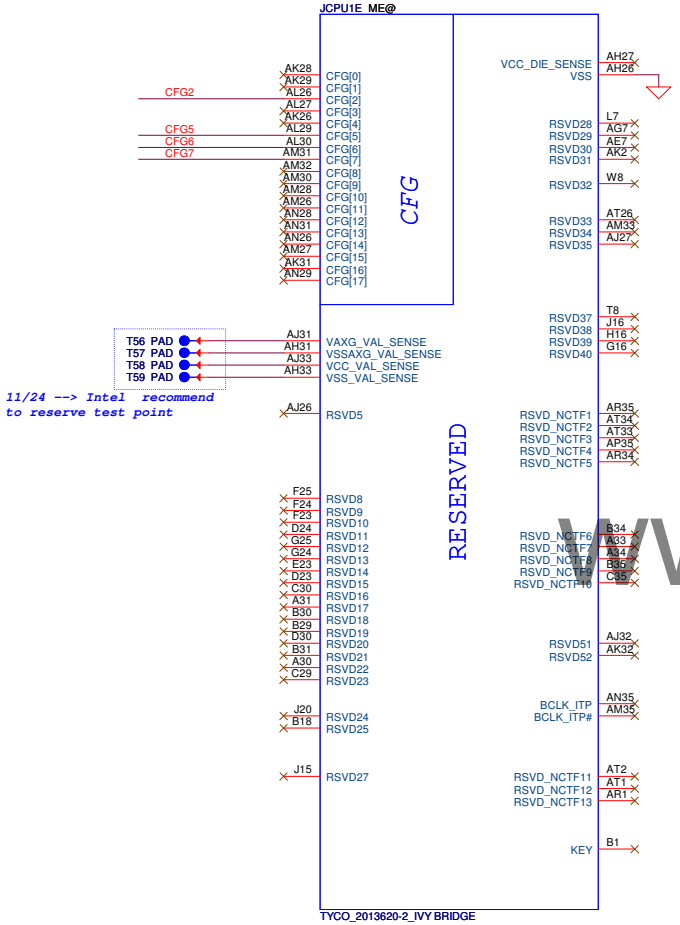
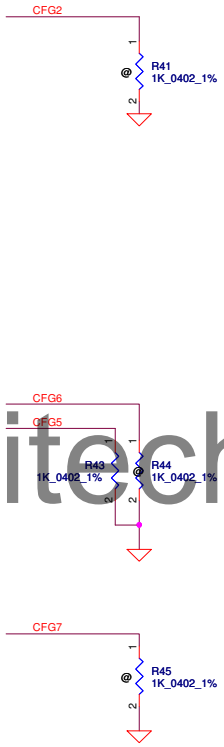


CFG Straps for Processor



PEG Static Lane Reversal – CFG2 is for the 16x	
CFG2	* 1: Normal Operation; Lane # definition matches socket pin map definition 0:Lane Reversed

Display Port Presence Strap	
CFG4	* 1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port

PCIE Port Bifurcation Straps	
CFG[6:5]	* 11: (Default) x16 – Device 1 functions 1 and 2 disabled 10: x8, x8 – Device 1 function 1 enabled ; function 2 disabled 01: Reserved – (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 – Device 1 functions 1 and 2 enabled

PEG DEFER TRAINING	
CFG7	1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training

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Title: PROCESSOR(4/7) RSVD,CFG

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POWER

JCPU1F ME@

+VCC_CORE

QC=94A
DC=53A

+1.05VS

8.5A

CORE SUPPLY

AG35	VCC1	AH13	VCCIO1
AG34	VCC2	AH10	VCCIO2
AG33	VCC3	AG10	VCCIO3
AG32	VCC4	AC10	VCCIO4
AG31	VCC5	Y10	VCCIO5
AG30	VCC6	U10	VCCIO6
AG29	VCC7	P10	VCCIO7
AG28	VCC8	L10	VCCIO8
AG27	VCC9	J14	VCCIO9
AG26	VCC10	J13	VCCIO10
AF35	VCC11	J12	VCCIO11
AF34	VCC12	J11	VCCIO12
AF33	VCC13	H14	VCCIO13
AF32	VCC14	H12	VCCIO14
AF31	VCC15	H11	VCCIO15
AF30	VCC16	G14	VCCIO16
AF29	VCC17	G13	VCCIO17
AF28	VCC18	G12	VCCIO18
AF27	VCC19	F14	VCCIO19
AF26	VCC20	F13	VCCIO20
AD35	VCC21	F12	VCCIO21
AD34	VCC22	F11	VCCIO22
AD33	VCC23	E14	VCCIO23
AD32	VCC24	E12	VCCIO24
AD31	VCC25	E11	
AD30	VCC26	D14	VCCIO25
AD29	VCC27	D13	VCCIO26
AD28	VCC28	D12	VCCIO27
AD27	VCC29	D11	VCCIO28
AD26	VCC30	C14	VCCIO29
AC35	VCC31	C13	VCCIO30
AC34	VCC32	C12	VCCIO31
AC33	VCC33	C11	VCCIO32
AC32	VCC34	B14	VCCIO33
AC31	VCC35	B12	VCCIO34
AC30	VCC36	A14	VCCIO35
AC29	VCC37	A13	VCCIO36
AC28	VCC38	A12	VCCIO37
AC27	VCC39	A11	VCCIO38
AC26	VCC40		VCCIO39
AA35	VCC41	J23	VCCIO40
AA34	VCC42		
AA33	VCC43		
AA32	VCC44		
AA31	VCC45		
AA30	VCC46		
AA29	VCC47		
AA28	VCC48		
AA27	VCC49		
AA26	VCC50		
Y35	VCC51		
Y34	VCC52		
Y33	VCC53		
Y32	VCC54		
Y31	VCC55		
Y30	VCC56		
Y29	VCC57		
Y28	VCC58		
Y27	VCC59		
Y26	VCC60		
V35	VCC61		
V34	VCC62		
V33	VCC63		
V32	VCC64		
V31	VCC65		
V30	VCC66		
V29	VCC67		
V28	VCC68		
V27	VCC69		
V26	VCC70		
U35	VCC71		
U34	VCC72		
U33	VCC73		
U32	VCC74		
U31	VCC75		
U30	VCC76		
U29	VCC77		
U28	VCC78		
U27	VCC79		
U26	VCC80		
R35	VCC81		
R34	VCC82		
R33	VCC83		
R32	VCC84		
R31	VCC85		
R30	VCC86		
R29	VCC87		
R28	VCC88		
R27	VCC89		
R26	VCC90		
P35	VCC91		
P34	VCC92		
P33	VCC93		
P32	VCC94		
P31	VCC95		
P30	VCC96		
P29	VCC97		
P28	VCC98		
P27	VCC99		
P26	VCC100		

PEG AND DDR

SVID

+1.05VS

C36 @ 0.1U_0402_10V7K

R46 75_0402_5%

Reserve 0.1u to avoid noise

Place the PU resistor close to CPU

VIDALERT#	AJ29	H_CPU_SVIDALRT#	R47	43_0402_5%	VR_SVID_ALRT# <59>
VIDSCLK	AJ30	H_CPU_SVIDCLK	R48	0_0402_5%	VR_SVID_CLK <59>
VIDSOUT	AJ28	H_CPU_SVIDDAT	R49	0_0402_5%	VR_SVID_DAT <59>

R50 130_0402_5% +1.05VS

Place the PU resistor close to CPU

SENSE LINES

+VCC_CORE

R51 100_0402_1%

VCC_SENCE 100ohm +-1% pull-up to VCC near processor

VCC_SENSE	AJ35	VCCSENSE_R	R52	0_0402_5%	VCCSENSE	VCCSENSE <59>
VSS_SENSE	AJ34	VSSSENSE_R	R53	0_0402_5%	VSSSENSE	VSSSENSE <59>

+1.05VS

R1294 10_0402_1%

VCCIO_SENSE	B10	VCCIO_SENSE			VCCIO_SENSE <57>
VSS_SENSE_VCCIO	A10	VSSIO_SENSE			

R1297 10_0402_1%

R54 100_0402_1%

VSS_SENCE 100ohm +-1% pull-down to GND near processor

TYCO_2013620-2_IVY BRIDGE

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Compal Electronics, Inc.

Title: PROCESSOR(5/7) PWR,BYPASS

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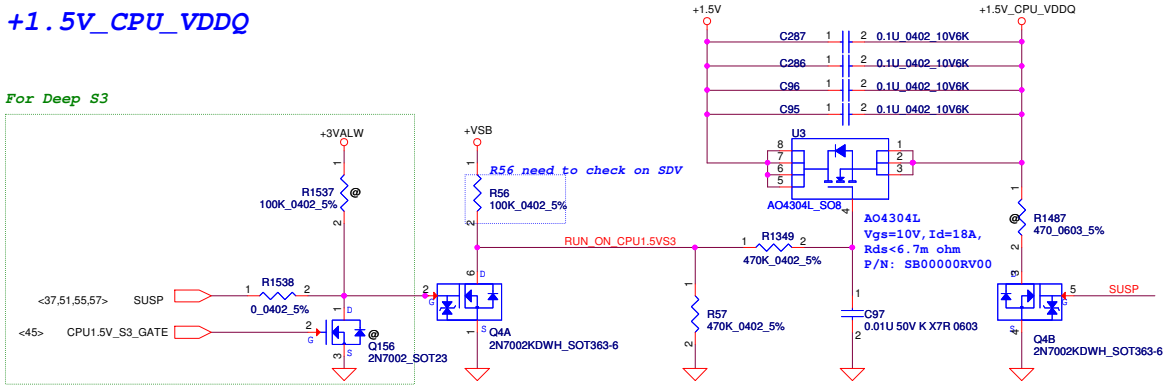
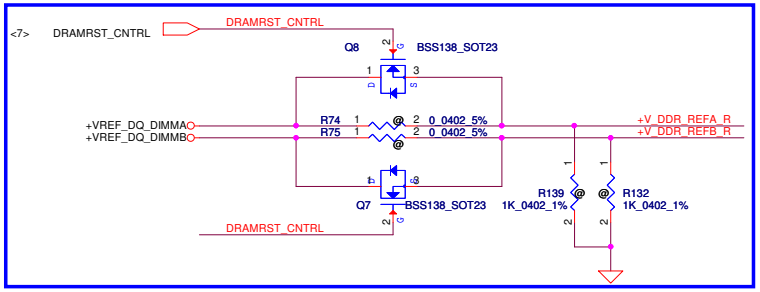
+1.5V_CPU_VDDQ

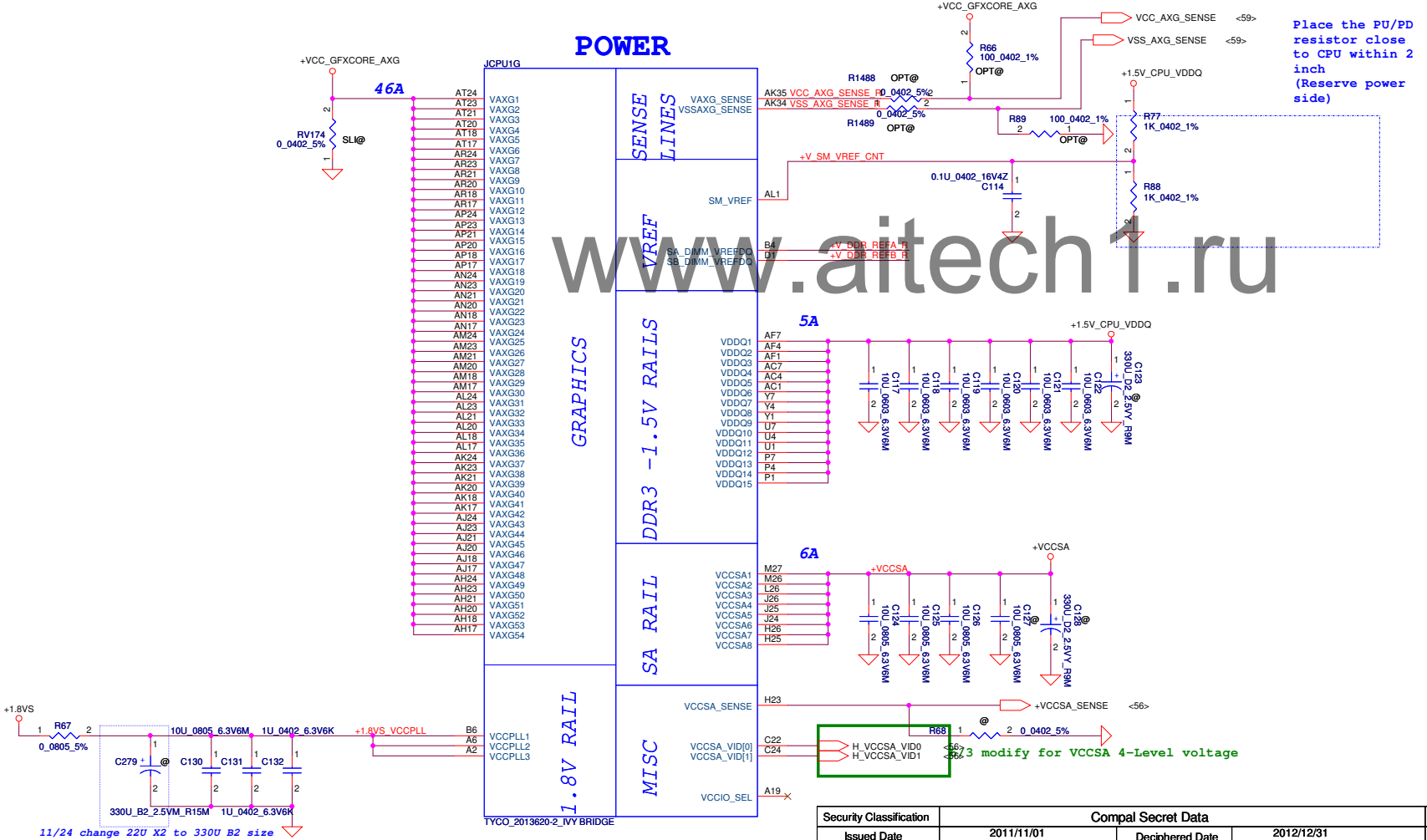
For Deep S3





6/8: Add M3 Circuit (Processor Generated SO-DIMM VREF_DQ)

POWER



Place the PU/PD resistor close to CPU within 2 inch (Reserve power side)

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Title: **PROCESSOR(6/7) PWR**

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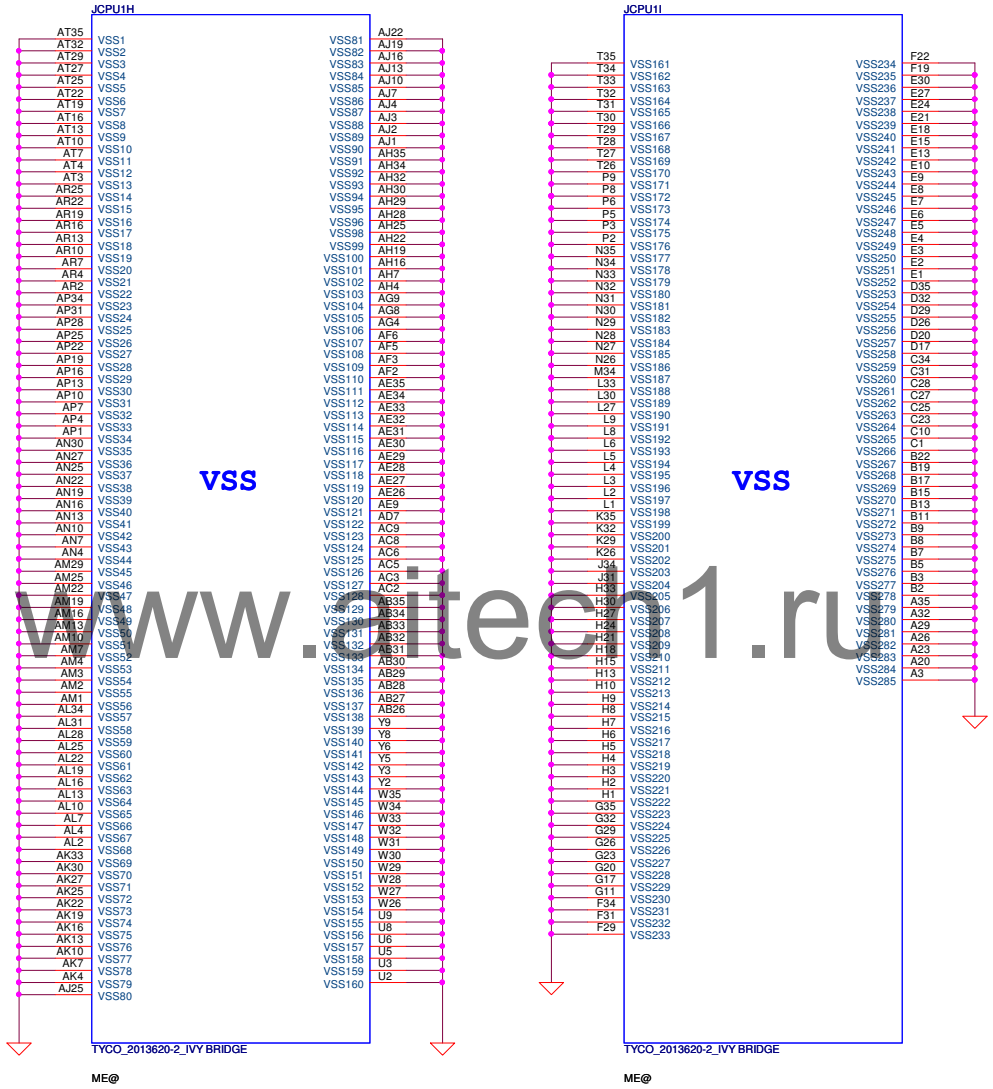

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Title: PROCESSOR(7/7) VSS

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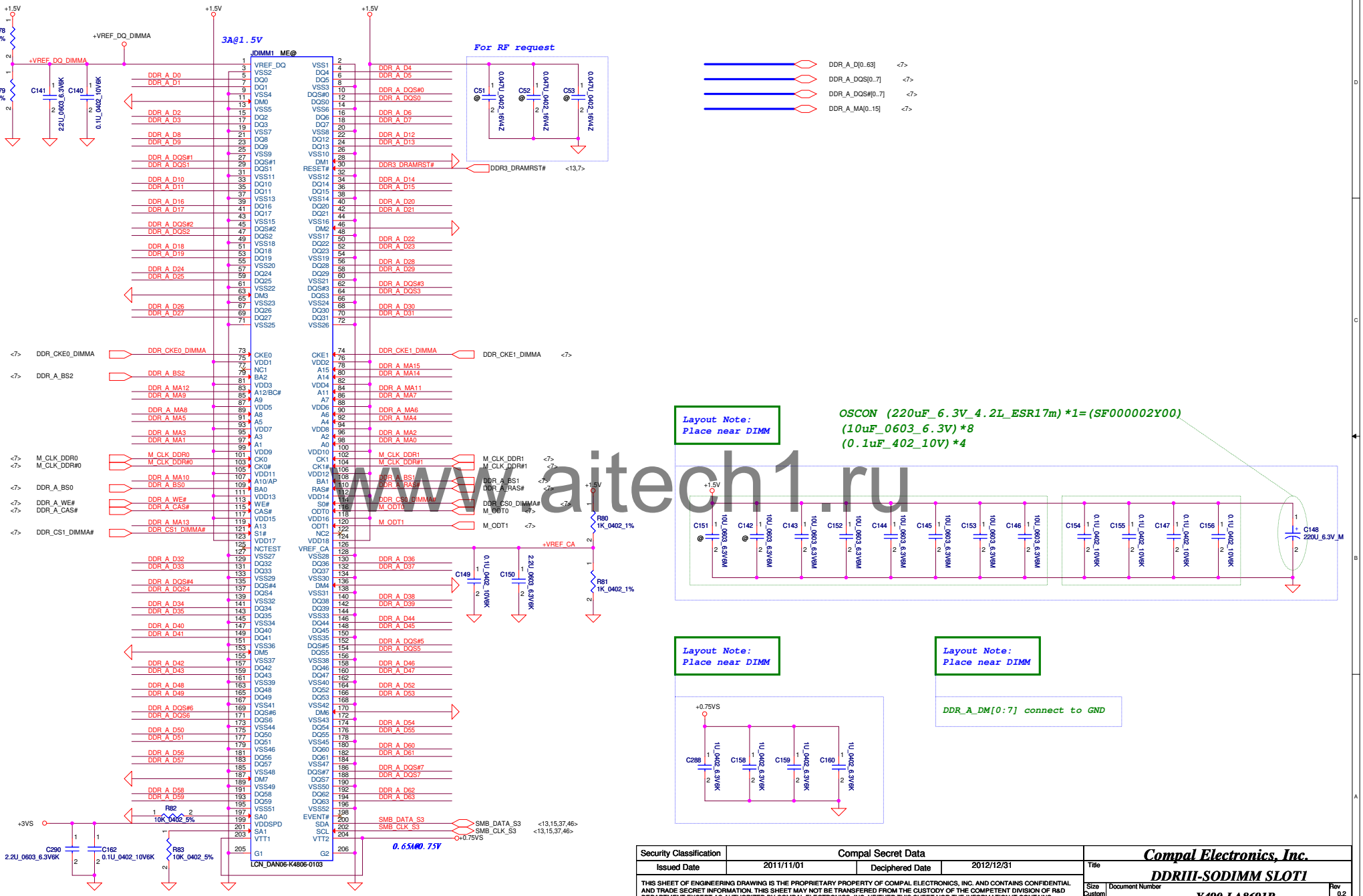
DDR3 SO-DIMM A



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Title: DDRIII-SODIMM SLOT1

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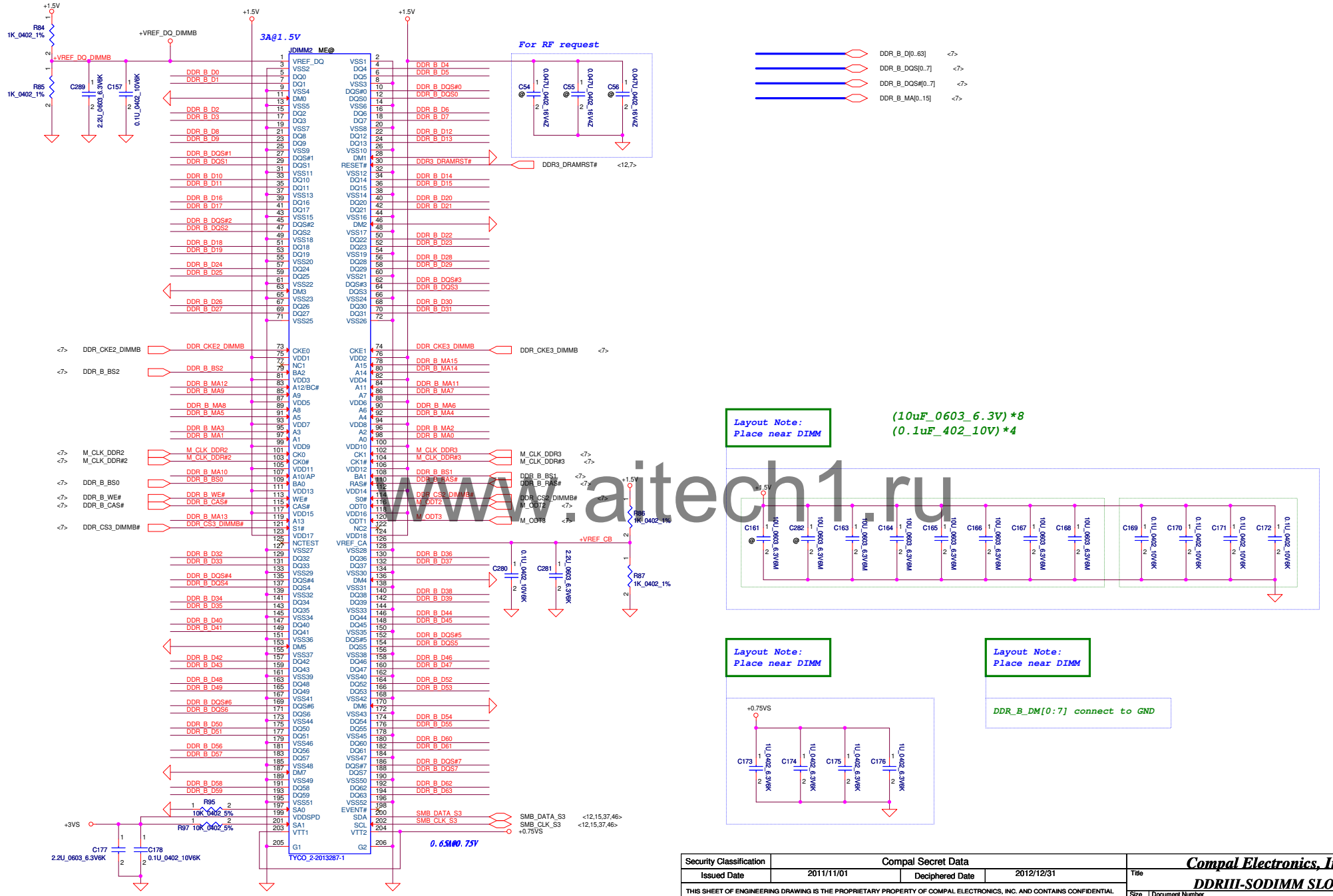
DDR3 SO-DIMM B



Layout Note: Place near DIMM

(10uF_0603_6.3V)*8
(0.1uF_402_10V)*4

Layout Note: Place near DIMM

Layout Note: Place near DIMM

DDR_B_DM[0:7] connect to GND

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Title	DDRIII-SODIMM SLOT2		
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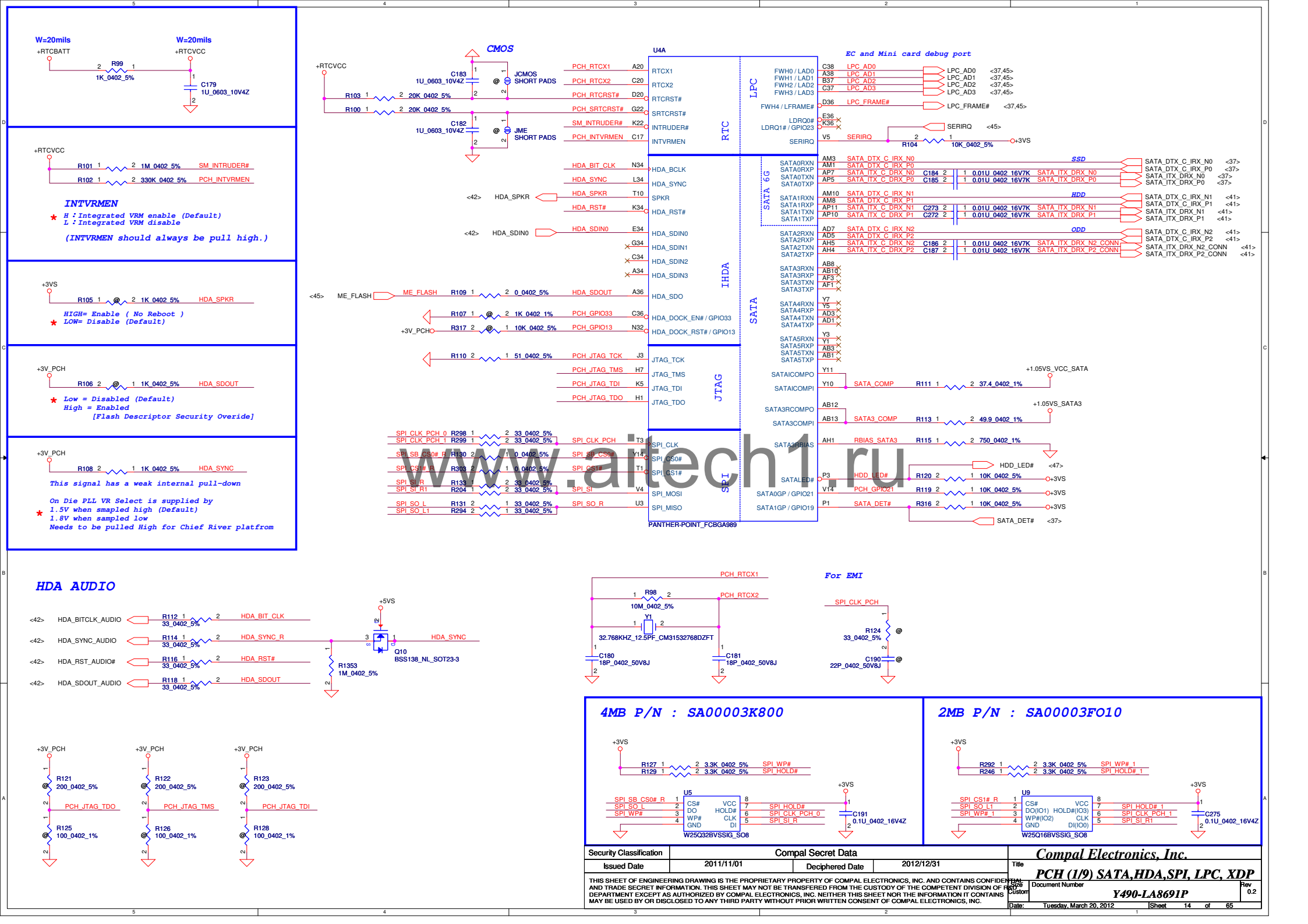
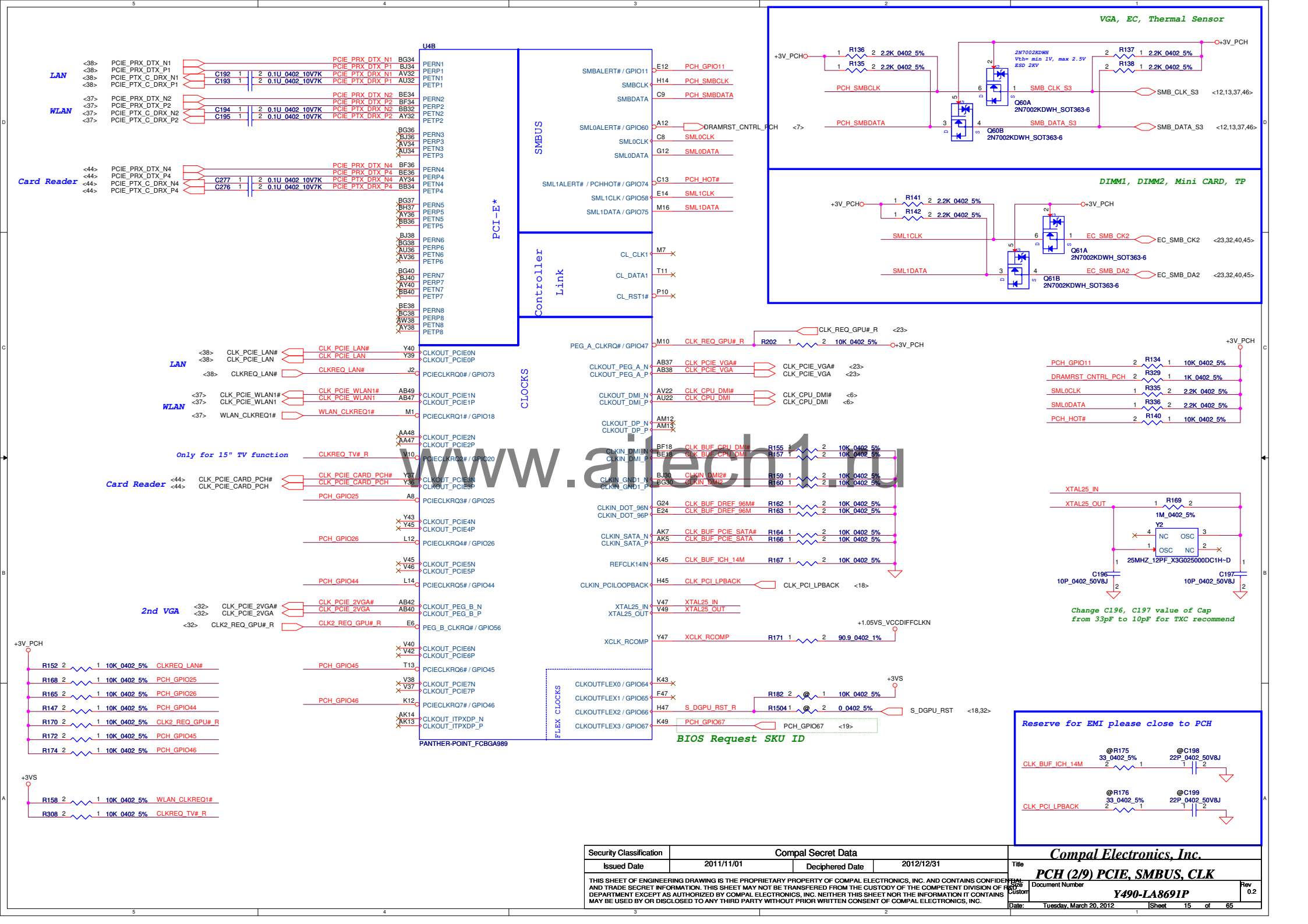
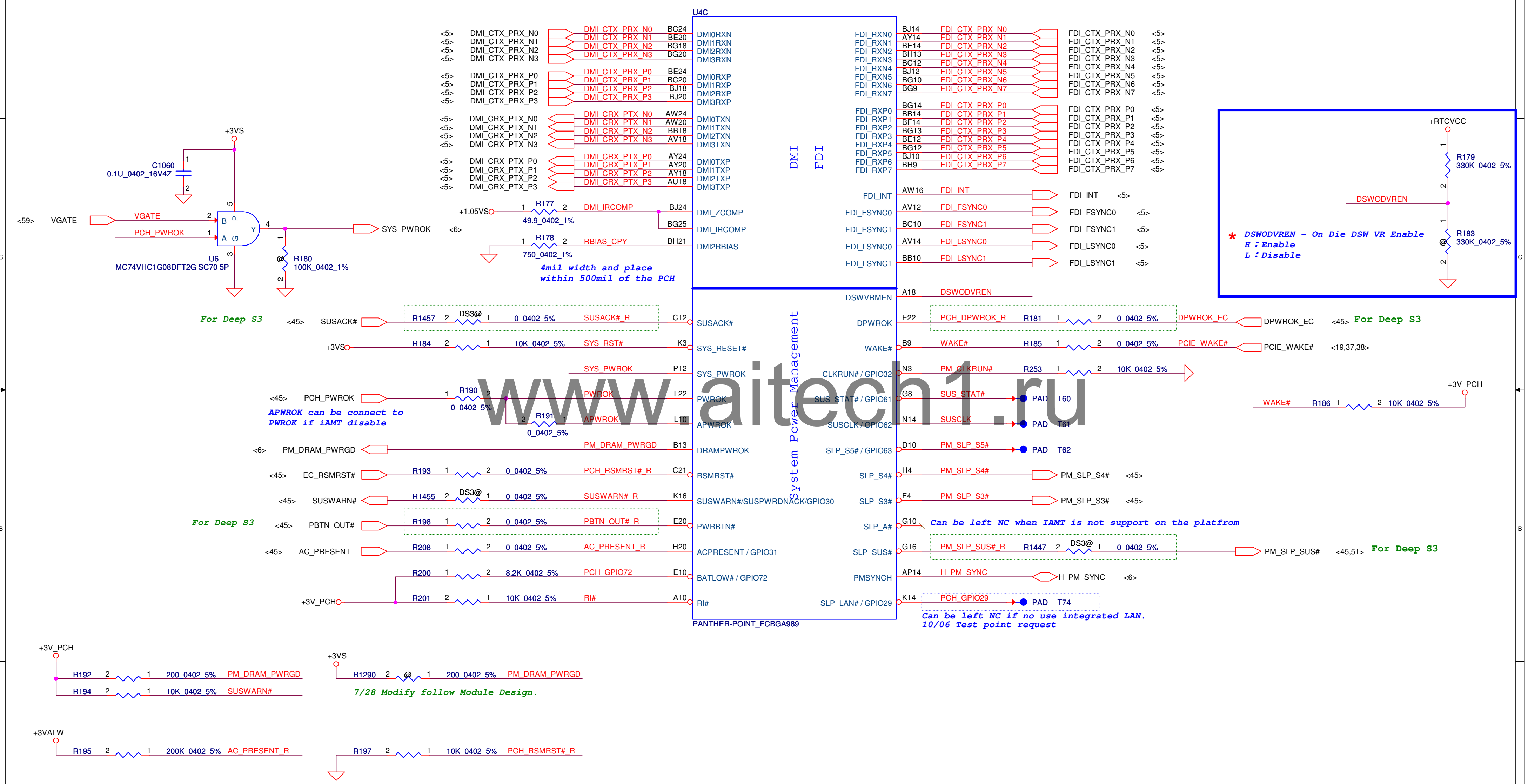




Security Classification	Compal Secret Data		
Issued Date	2011/11/01	Deciphered Date	2012/12/31

Compal Electronics, Inc.			
Title: PCH (2/9) PCIE, SMBUS, CLK			
Size: Custom	Document Number: Y490-LA8691P		Rev: 0.2
Date: Tuesday, March 20, 2012	Sheet 15 of 65		



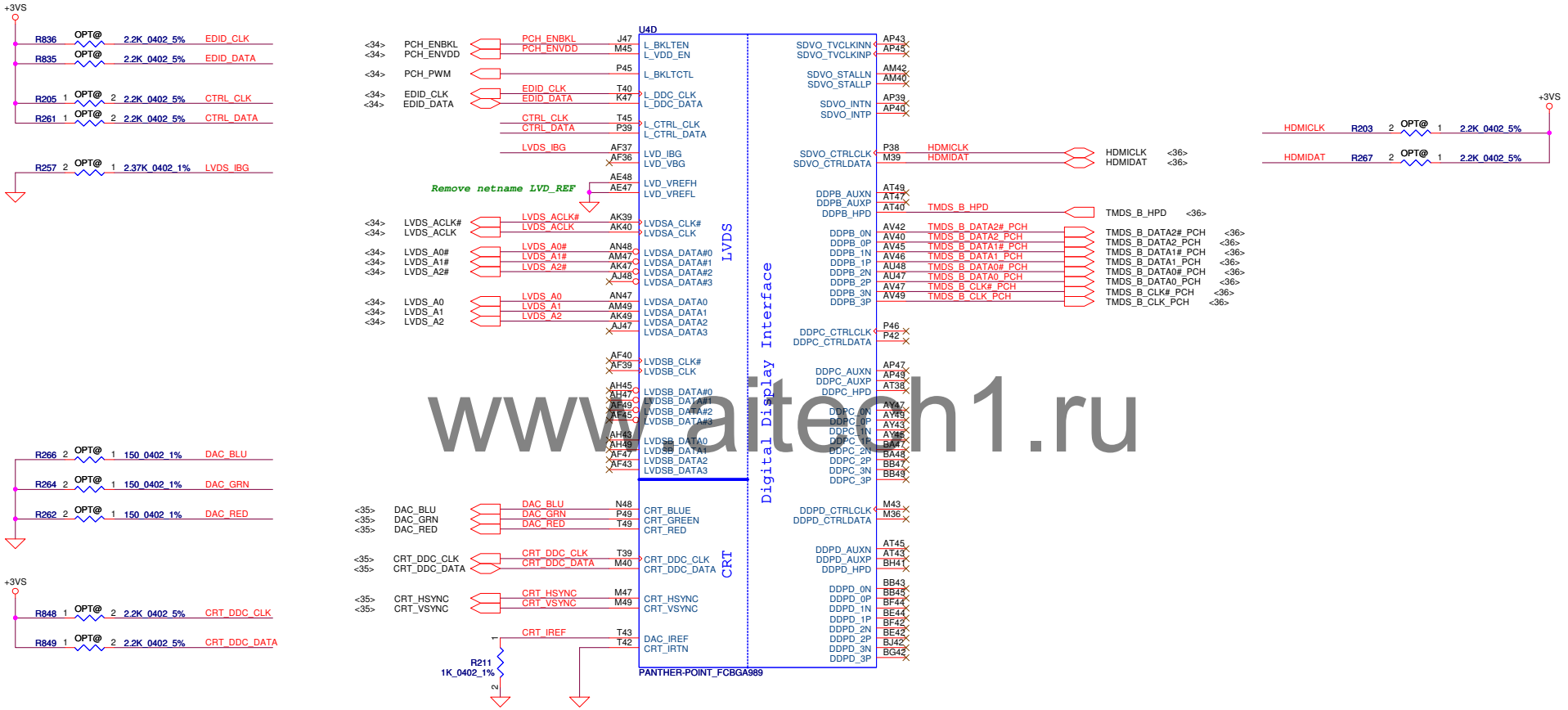
Security Classification	Compal Secret Data		
Issued Date	2011/11/01	Deciphered Date	2012/12/31

Compal Electronics, Inc.

Title: PCH (3/9) DMI,FDI,PM,

Size: Custom | Document Number: Y490-LA8691P | Rev: 0.2

Date: Tuesday, March 20, 2012 | Sheet 16 of 65

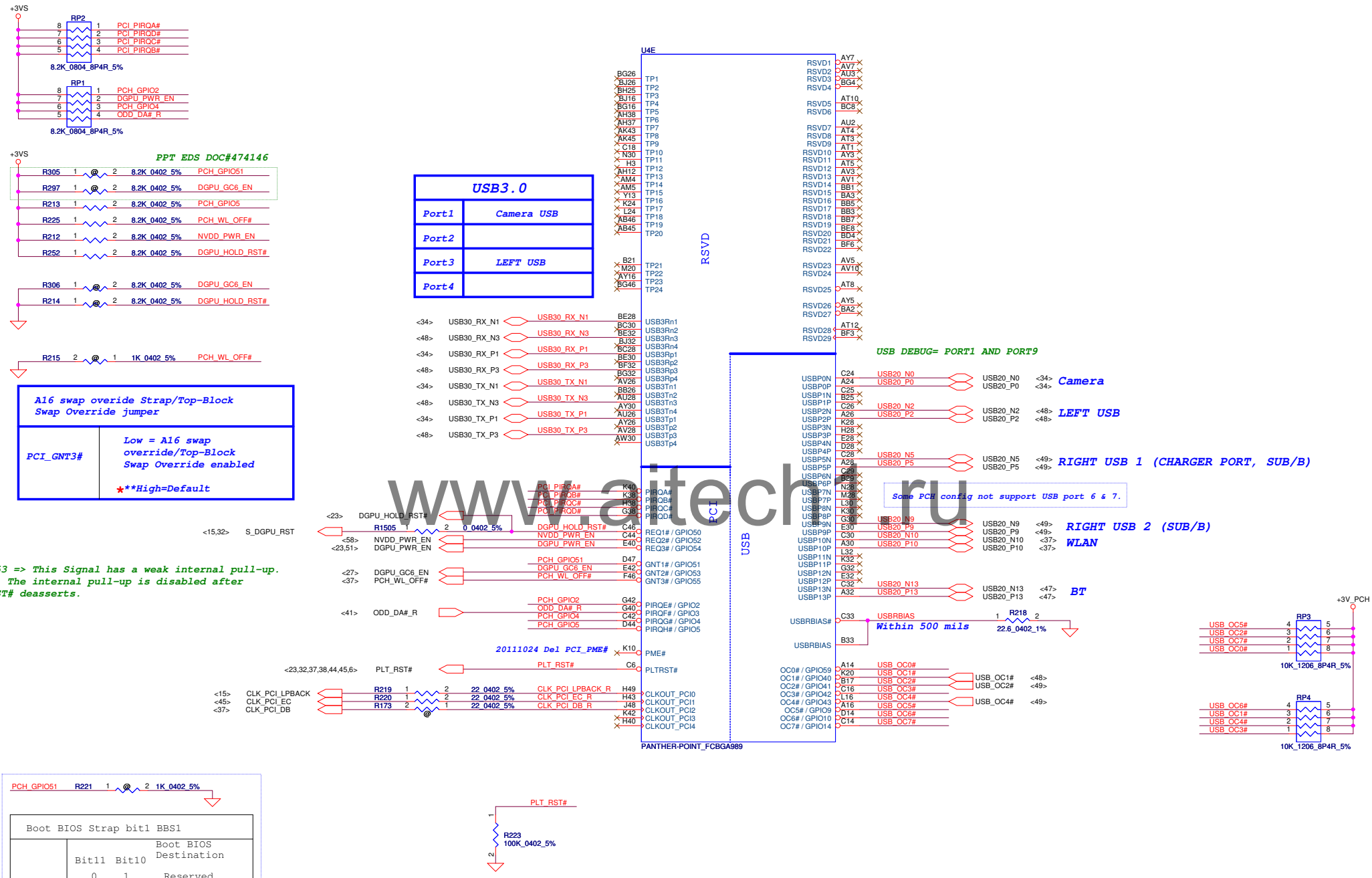


Security Classification	Compal Secret Data		
Issued Date	2011/11/01	Deciphered Date	2012/12/31

Title: PCH (4/9) LVDS,CRT,DP,HDMI

Size	Document Number	Rev
Custom	Y490-LA8691P	0.2

Date: Tuesday, March 20, 2012 Sheet 17 of 65



Security Classification	Compal Secret Data		
Issued Date	2011/11/01	Deciphered Date	2012/12/31

Compal Electronics, Inc.

Title: PCH (5/9) PCI, USB

Size: Custom | Document Number: Y490-LA8691P | Rev: 0.2

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Function	PCH_GPIO38	PCH_GPIO67	PCH_GPIO70
Optimus	0	0	X
Reserve	0	1	X
DIS (SLI)	1	0	X
Reserve	1	1	X
14"	X	X	0
15"	X	X	1

SKU ID

+3VS
R711 SLI@ 10K_0402_5%
R708 @ 10K_0402_5%
R704 @ 10K_0402_5%
PCH_GPIO38
<15> PCH_GPIO67
PCH_GPIO67
PCH_GPIO70
R712 OPT@ 10K_0402_5%
R709 10K_0402_5%
R706 10K_0402_5%

+3VS
10K_0402_5% R1493 EC_SCI#
+3V_PCH
R235 10K_0402_5% EC_SMI#

GPIO28
On-Die PLL Voltage Regulator
This signal has a weak internal pull up
* H : On-Die voltage regulator enable
L : On-Die PLL Voltage Regulator disable
R240 @ 1K_0402_5% PCH_GPIO28

* PCH_GPIO27 (Have internal Pull-High)
High: VCCVRM VR Enable
Low: VCCVRM VR Disable

+3VALW
DS3@ R207 10K_0402_5%
R245 @ 10K_0402_5% DS3_WAKE#_R

+3VS
200K_0402_5% R250 ODD_DETECT#
+3V_PCH
10K_0402_5% R251 SLAVE_PRESENT#
R259 10K_0402_5% PCH_GPIO37

<23,32> GC6_EVENT# GC6_EVENT#
+3VS R233 10K_0402_5%

U4F

T7	BMBUSY# / GPIO0	TACH4 / GPIO68	C40 PCH_GPIO68
R227 PCH_GPIO1	A42 TACH1 / GPIO1	TACH5 / GPIO69	B41 S_DGPU_PWR_EN → S_DGPU_PWR_EN <32,51>
R228 PCH_GPIO6	H36 TACH2 / GPIO6	TACH6 / GPIO70	C41 PCH_GPIO70 9/18 Reseve for SKU ID
<45> EC_SCI# EC_SCI#	E38 TACH3 / GPIO7	TACH7 / GPIO71	A40 S_NVDD_PWR_EN → S_NVDD_PWR_EN <32>
<45> EC_SMI# EC_SMI#	C10 GPIO8		
R229 @ PCH_GPIO12	C4 LAN_PHY_PWR_CTRL / GPIO12		
R230 EC_LID_OUT#	G2 GPIO15	A20GATE	P4 R236 10K_0402_5% +3VS GATEA20 <45>
<45> EC_LID_OUT#		PECI	AU16
R231 PCH_GPIO16	U2 SATA4GP / GPIO16	RCIN#	P5 KBRST# KBRST# <45>
R232 @ 10K_0402_1%		PROCPWRGD	AY11 H_CPUPWRGD <6>
<27,32,55,58> DGPU_PWROK	D40 TACH0 / GPIO17	THRMTRIP#	AY10 PCH_THRMTRIP#_R R239 390_0402_5% H_THRMTRIP# H_THRMTRIP# <6>
R238 PCH_BT_DISABLE#	T5 SCLOCK / GPIO22	INIT3_3V#	T14
<37> PCH_BT_DISABLE#		DF_TVS	AY1 NV_CLE → PCH_THRMTRIP#_R <23,32>
<41> ODD_EN ODD_EN	E8 GPIO24		
<16,37,38> PCIE_WAKE# 0_0402_5% R224	E16 GPIO27	TS_VSS1	AH8
R241 PCH_GPIO28	P8 GPIO28	TS_VSS2	AK11
<37,47> PCH_BT_ON#		TS_VSS3	AH10
+3VS R242 PCH_BT_ON#	K1 STP_PCI# / GPIO34	TS_VSS4	AK10
R243 PCH_GPIO35	K4 GPIO35	NC_1	P37
<41> ODD_DETECT# ODD_DETECT#	V8 SATA2GP / GPIO36		
PCH_GPIO37	M5 SATA3GP / GPIO37		
PCH_GPIO38	N2 SLOAD / GPIO38		
+3VS R247 PCH_GPIO39	M3 SDATAOUT0 / GPIO39		
R248 PCH_GPIO48	V13 SDATAOUT1 / GPIO48		
+3VS R249 PCH_GPIO49	V3 SATA5GP / GPIO49 / TEMP_ALERT#		
<32> SLAVE_PRESENT# SLAVE_PRESENT#	D6 GPIO57		

A4	VSS_NCTF_1	VSS_NCTF_15	BG2
A44	VSS_NCTF_2	VSS_NCTF_16	BG48
A45	VSS_NCTF_3	VSS_NCTF_17	BH3
A46	VSS_NCTF_4	VSS_NCTF_18	BH47
A5	VSS_NCTF_5	VSS_NCTF_19	BJ4
A6	VSS_NCTF_6	VSS_NCTF_20	BJ44
B3	VSS_NCTF_7	VSS_NCTF_21	BJ45
B47	VSS_NCTF_8	VSS_NCTF_22	BJ46
BD1	VSS_NCTF_9	VSS_NCTF_23	BJ5
BD49	VSS_NCTF_10	VSS_NCTF_24	BJ6
BE1	VSS_NCTF_11	VSS_NCTF_25	C2
BE49	VSS_NCTF_12	VSS_NCTF_26	C48
BF1	VSS_NCTF_13	VSS_NCTF_27	D1
BF49	VSS_NCTF_14	VSS_NCTF_28	D49
		VSS_NCTF_29	E1
		VSS_NCTF_30	E49
		VSS_NCTF_31	F1
		VSS_NCTF_32	F49

GPIO | CPU/MISC | NCTF

PANTHER-POINT_FCBGA989

S_DGPU_PWR_EN R268 10K_0402_5% +3VS
S_NVDD_PWR_EN R237 10K_0402_5% +3VS

INIT3_3V
This signal has weak internal PU, can't pull low

Intel schematic reviwe recommand.

PCH_GPIO68 R255 10K_0402_5%
KBRST# R226 10K_0402_5%
PCH_THRMTRIP#_R R244 10K_0402_5%
+3VS

PROC_SEL	H : Sandy Bridge
	L : IVY Bridge

+1.8VS
R216 2.2K_0402_5%
NV_CLE R217 1K_0402_5% H_SNB_IVB# <6>
CLOSE TO THE BRANCHING POINT

Security Classification	Compal Secret Data		
Issued Date	2011/11/01	Deciphered Date	2012/12/31

Compal Electronics, Inc.

Title: PCH (6/9) GPIO, CPU, MISC

Size	Document Number	Rev
Custom	Y490-LA8691P	0.2

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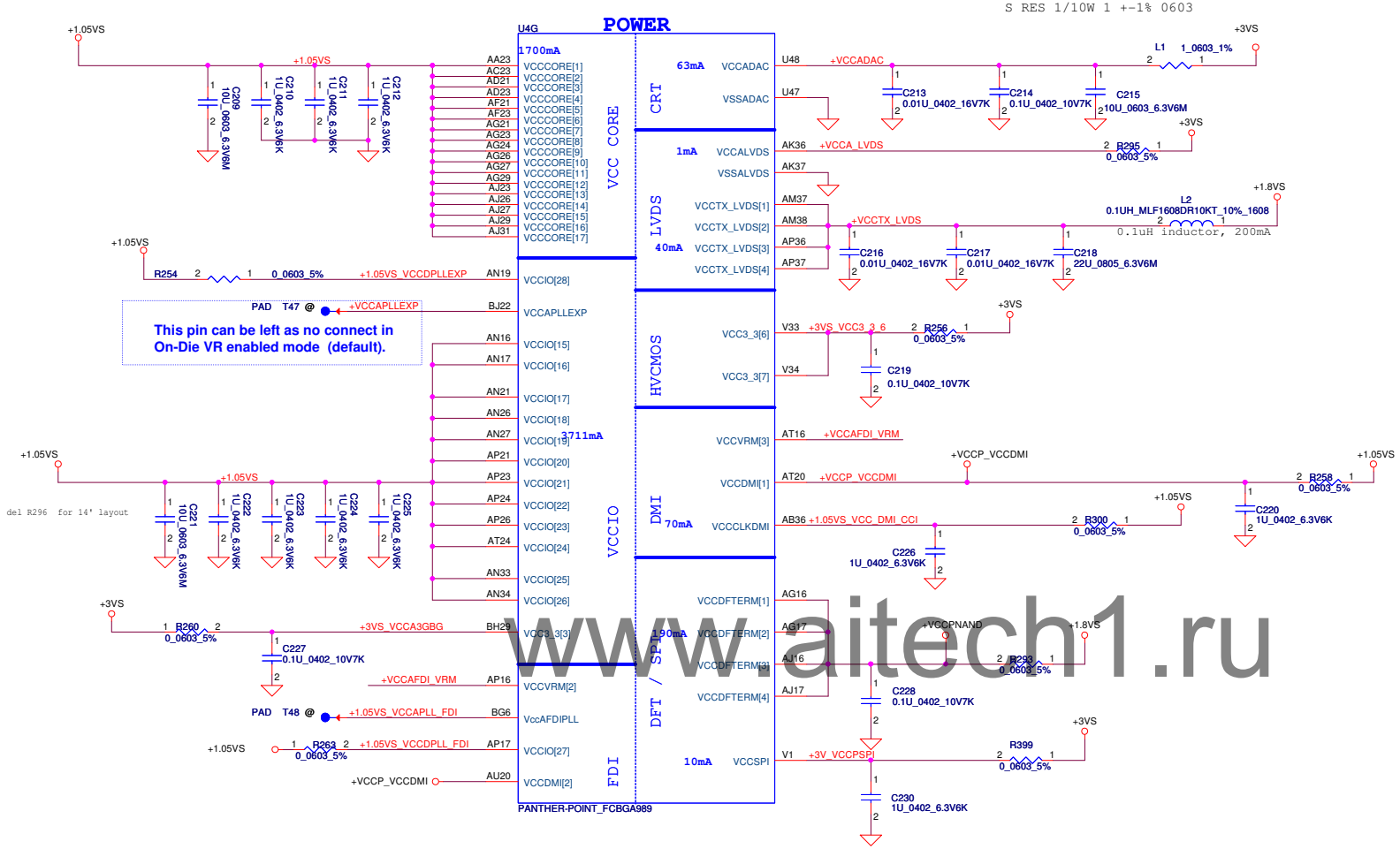


PCH Power Rail Table
Refer to CPU EDS R1.5

Voltage Rail	Voltage	S0 Iccmax Current (A)
V_PROC_IO	1.05	0.001
V5REF	5	0.001
V5REF_Sus	5	0.001
Vcc3_3	3.3	0.228
VccADAC	3.3	0.063
VccADPLLA	1.05	0.08
VccADPLLB	1.05	0.08
VccCore	1.05	1.7
VccDMI	1.05	0.047
VccIO	1.05	3.711
VccASW	1.05	0.903
VccSPI	3.3	0.01
VccDSW	3.3	0.001
VccDFTERM	1.8	0.002
VccRTC	3.3	6 uA
VccSus3_3	3.3	0.095
VccSusHDA	3.3 / 1.5	0.01
VccVRM	1.8 / 1.5	0.167
VccCLKDMI	1.05	0.07
VccSSC	1.05	0.095
VccDIFFCLKN	1.05	0.055
VccALVDS	3.3	0.001
VccTX_LVDS	1.8	0.04

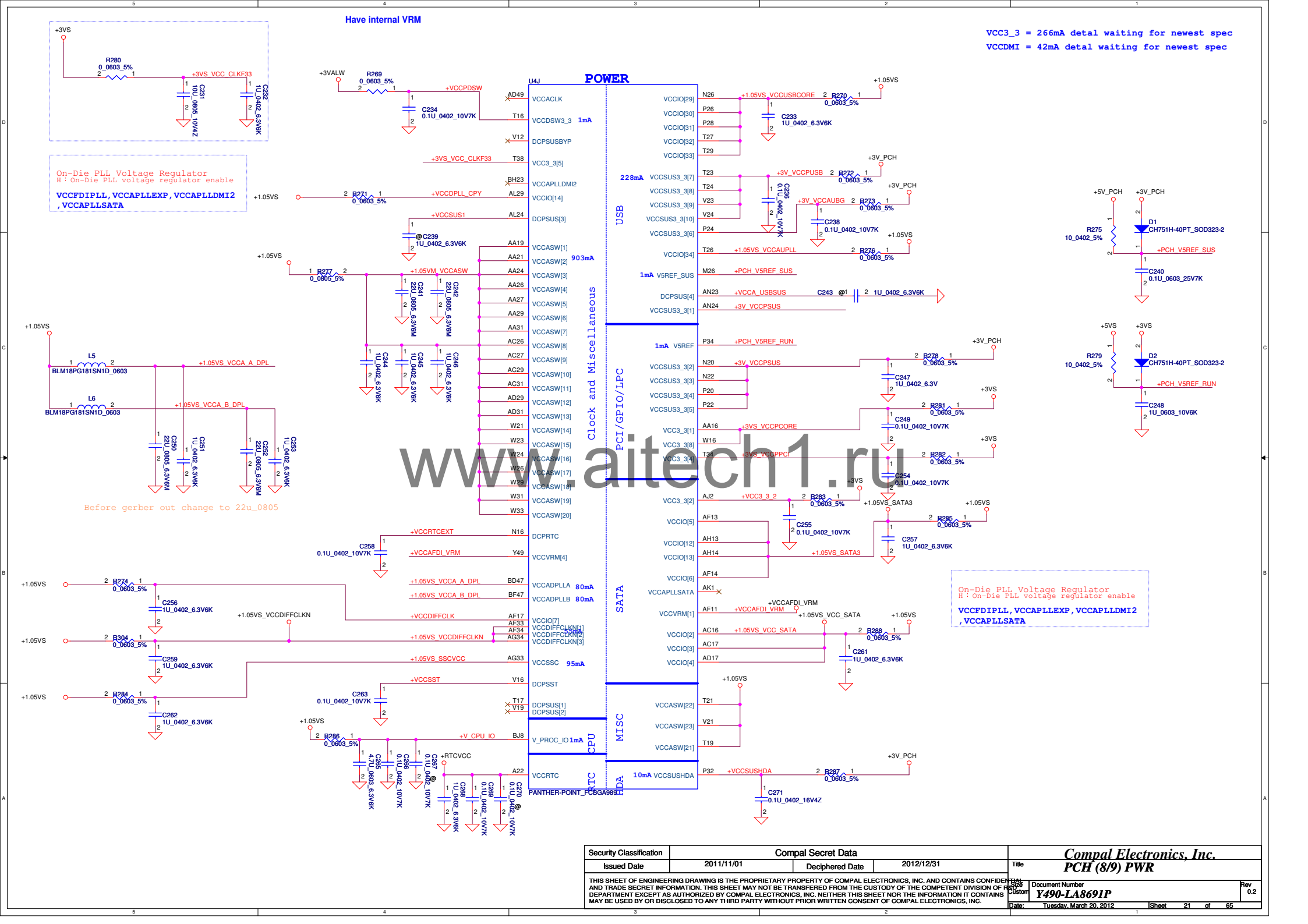
Security Classification	Compal Secret Data		
Issued Date	2011/11/01	Deciphered Date	2012/12/31

Compal Electronics, Inc.

Title: PCH (7/9) PWR

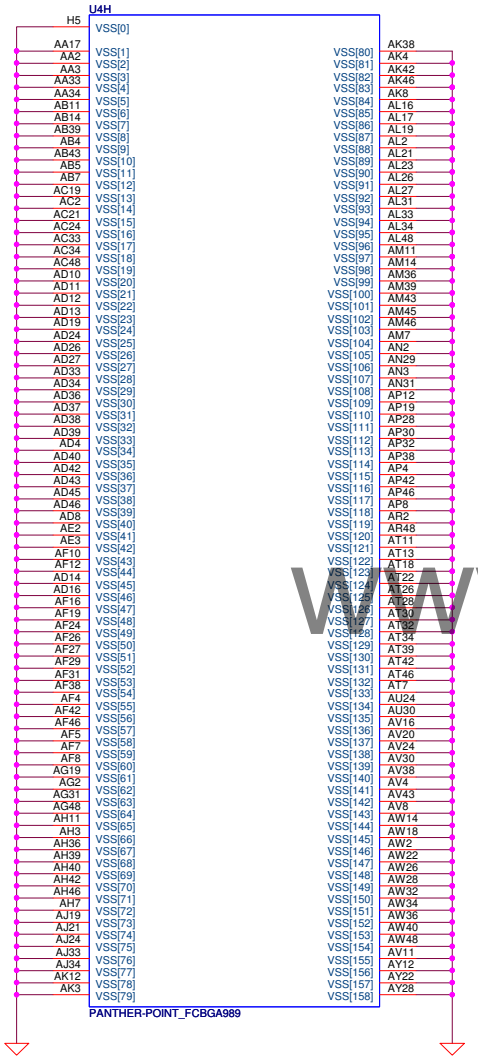
Size: Custom | Document Number: Y490-LA8691P | Rev: 0.2

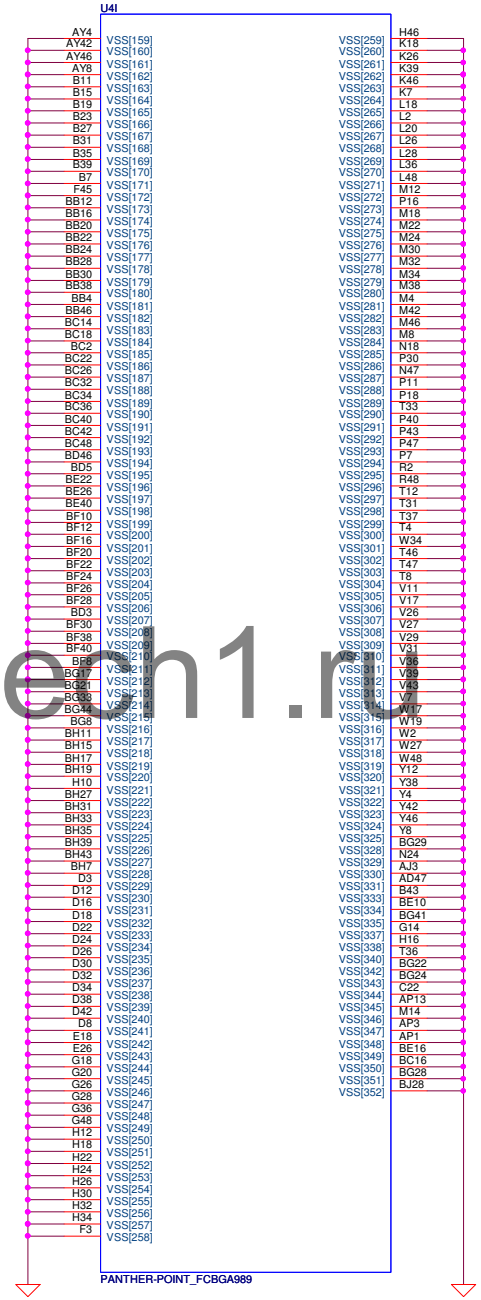
Date: Tuesday, March 20, 2012 | Sheet 20 of 65



Security Classification	Compal Secret Data		
Issued Date	2011/11/01	Deciphered Date	2012/12/31

Title	Compal Electronics, Inc. PCH (8/9) PWR		
Size: Custom	Document Number: Y490-LA8691P		Rev: 0.2
Date: Tuesday, March 20, 2012	Sheet 21 of 65		





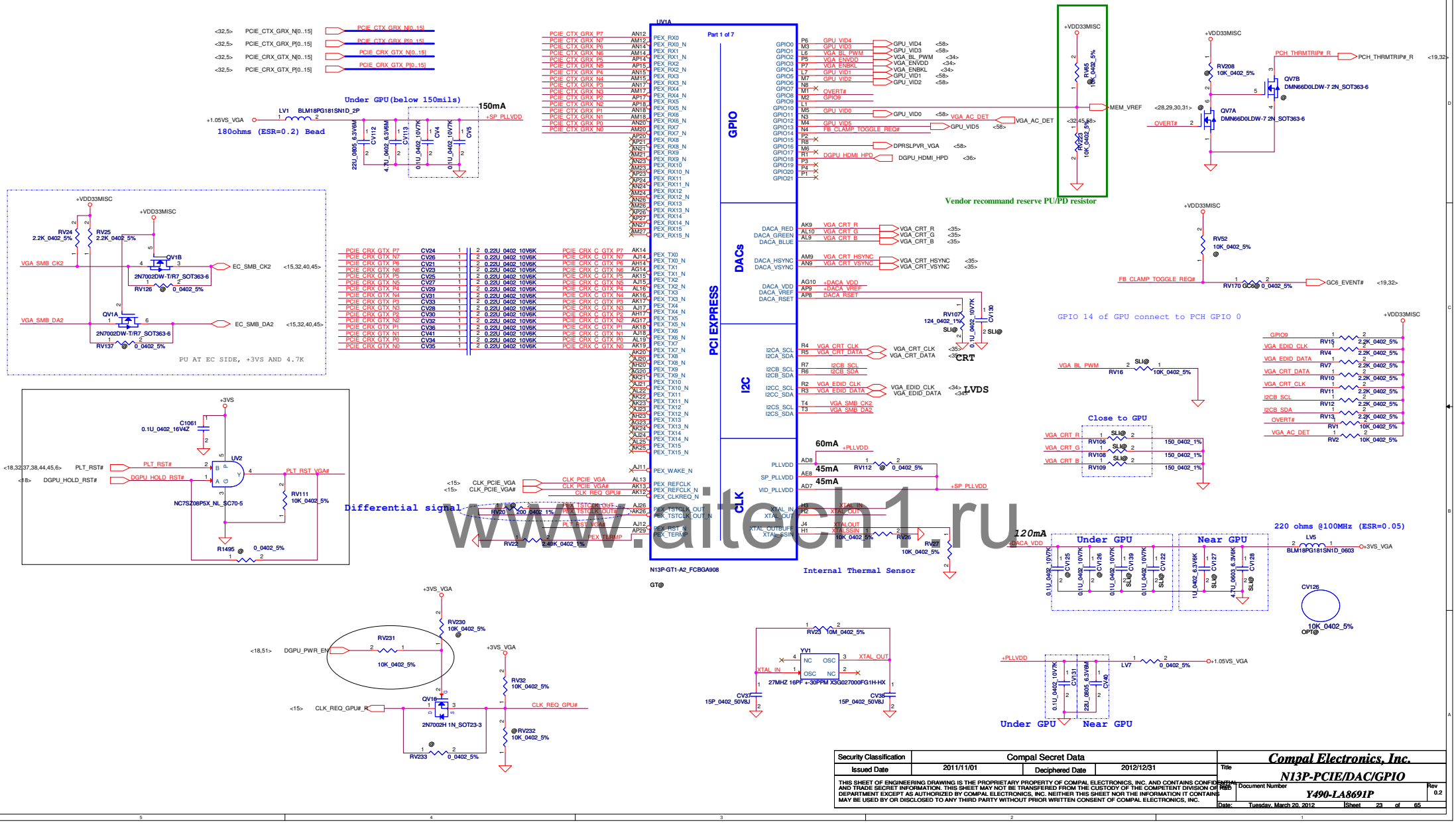
Security Classification	Compal Secret Data		
Issued Date	2011/11/01	Deciphered Date	2012/12/31

Compal Electronics, Inc.

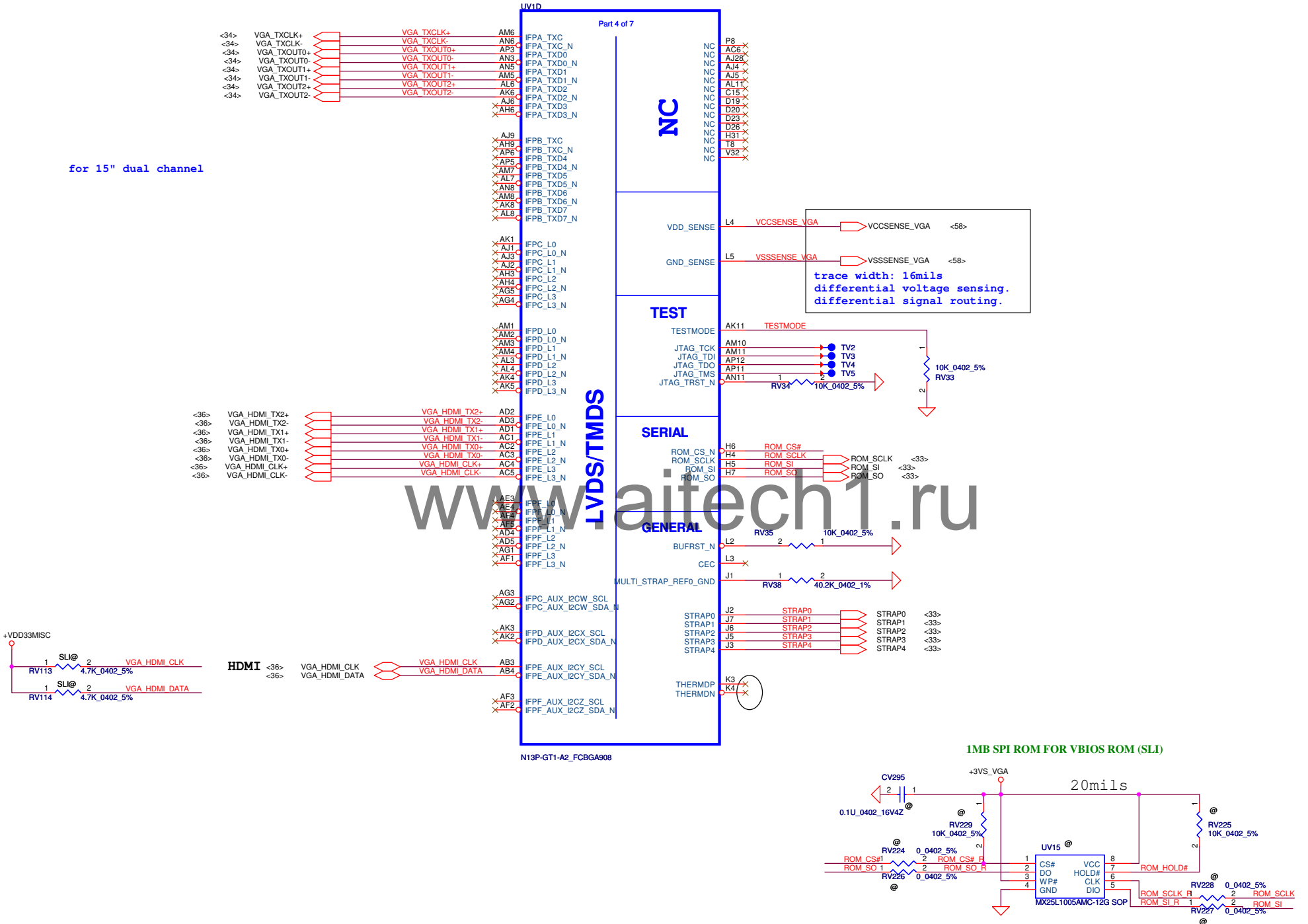
Title: PCH (9/9) VSS

Size: Custom | Document Number: Y490-LA8691P | Rev: 0.2

Date: Tuesday, March 20, 2012 | Sheet 22 of 65

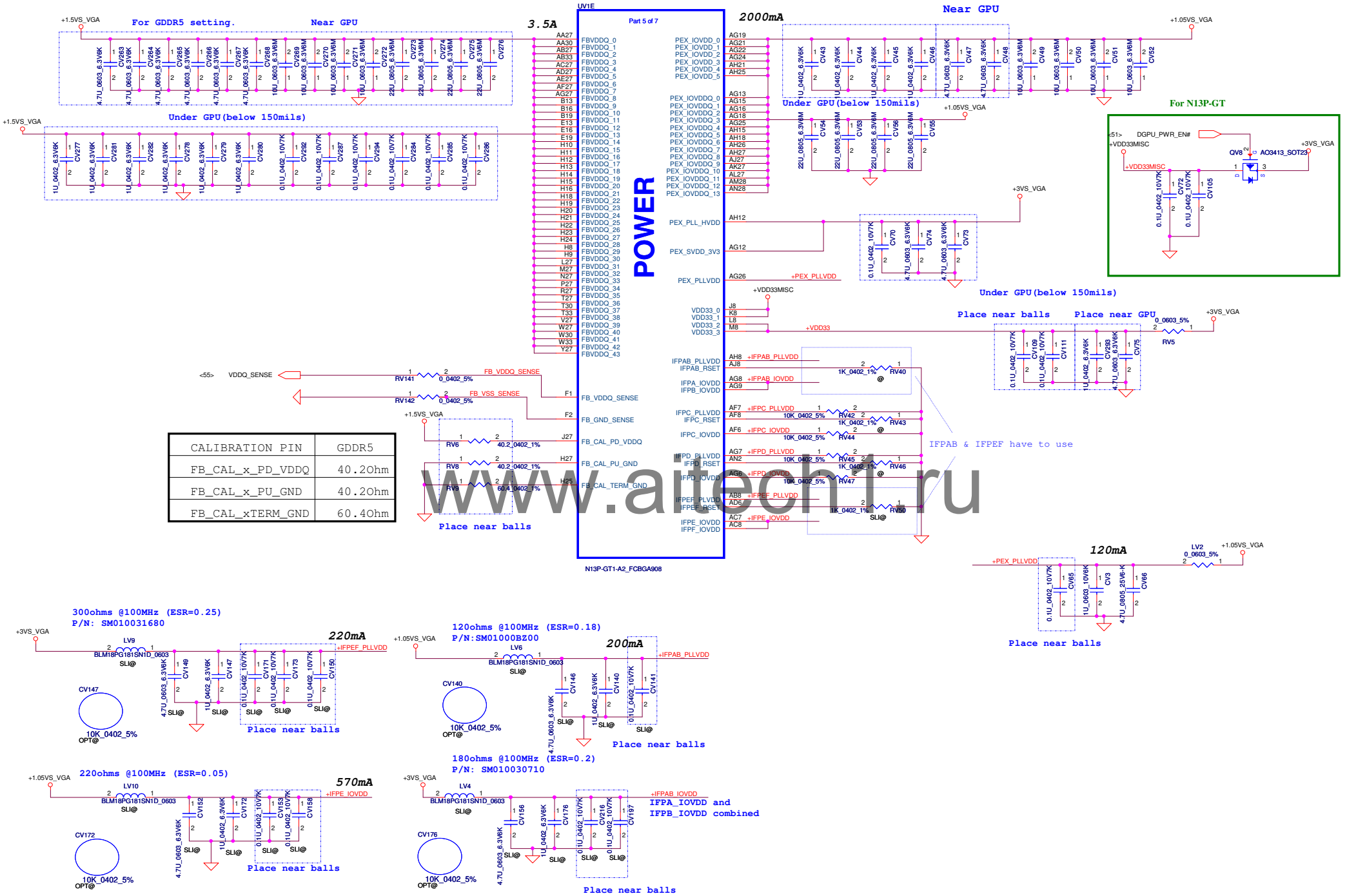


Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2011/11/01	Deciphered Date	2012/12/31
Title	N13P-PCIE/DAC/GPIO		
Document Number	Y490-LA8691P		Rev 0.2
Date: Tuesday, March 20, 2012	Sheet 23 of 65		



Security Classification	Compal Secret Data		
Issued Date	2011/11/01	Deciphered Date	2012/12/31

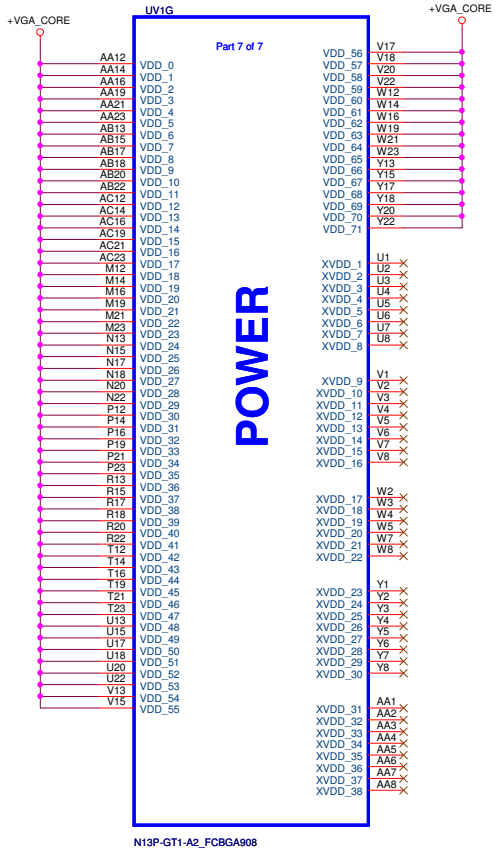
Compal Electronics, Inc.			
Title	N13P-LVDS/HDMI/DP/THM		
Size	Document Number	Y490-LA8691P	Rev 0.2
Date: Tuesday, March 20, 2012	Sheet 24 of 65		

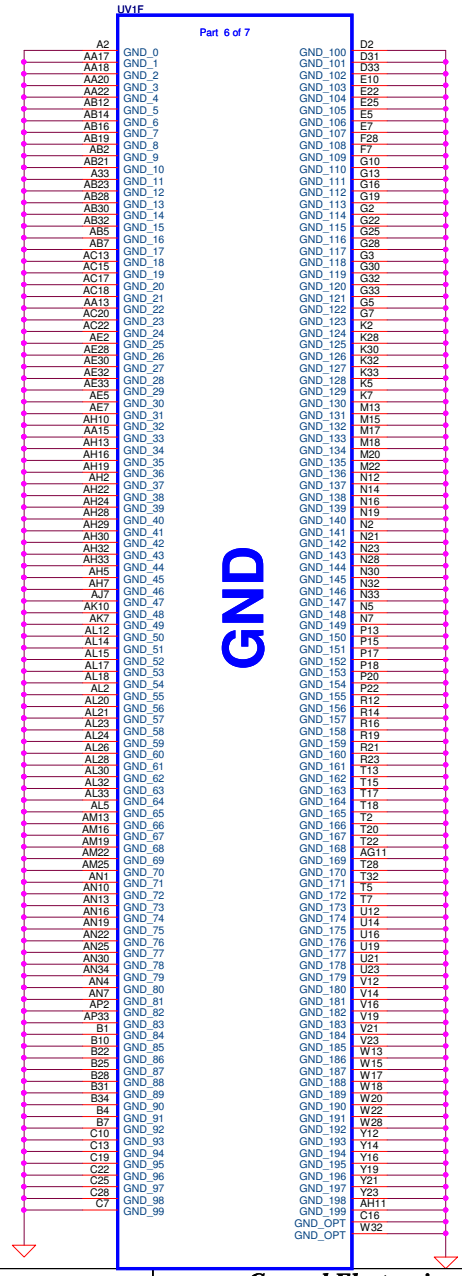


CALIBRATION PIN	GDDR5
FB_CAL_x_PD_VDDQ	40.2Ohm
FB_CAL_x_PU_GND	40.2Ohm
FB_CAL_xTERM_GND	60.4Ohm

Security Classification	Compal Secret Data		
Issued Date	2011/11/01	Deciphered Date	2012/12/31

Compal Electronics, Inc.			
Title: N13P-POWER			
Size	Document Number: Y490-LA8691P		Rev: 0.2
Date: Tuesday, March 20, 2012	Sheet 25 of 65		





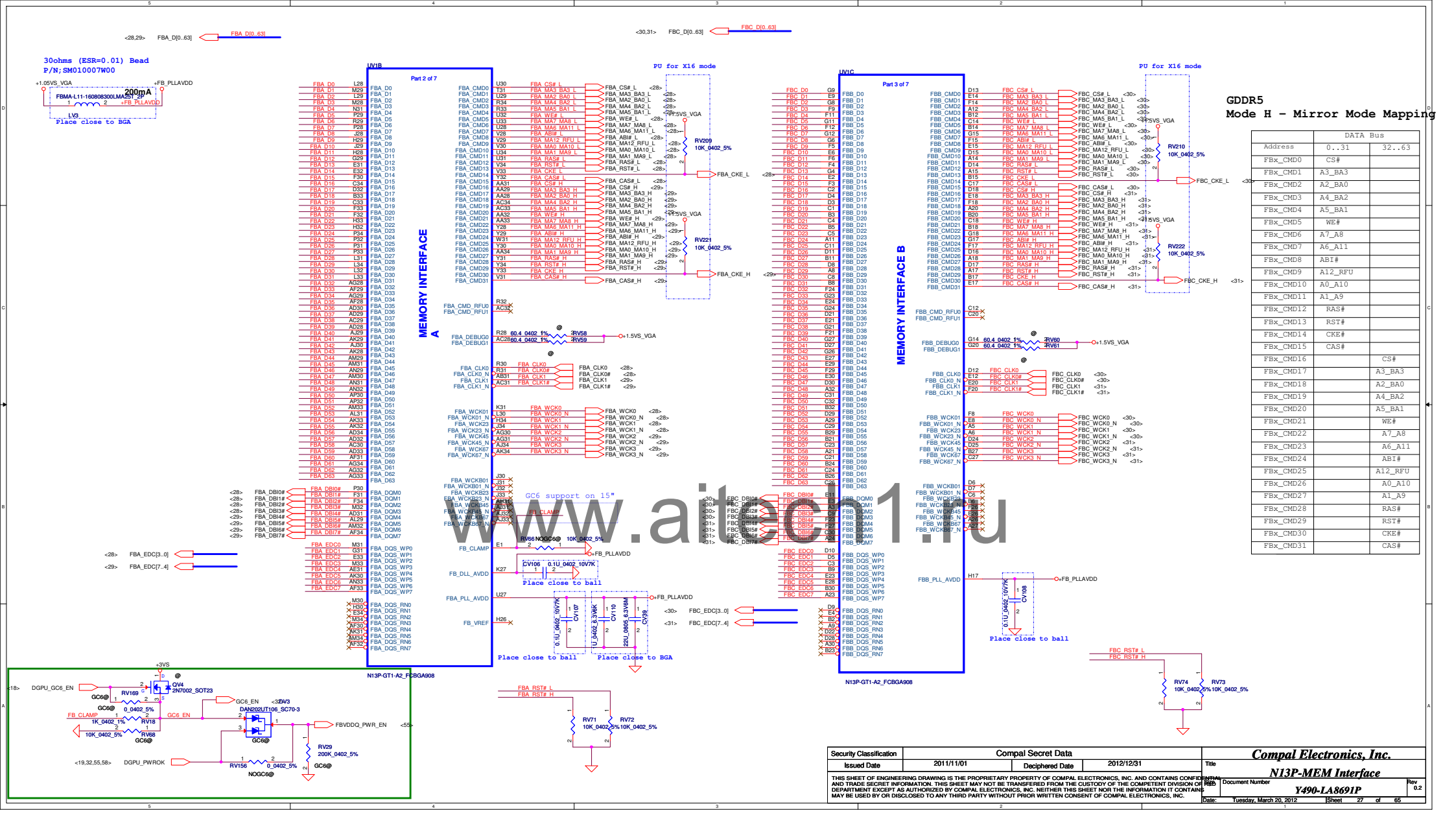
Security Classification	Compal Secret Data		
Issued Date	2011/11/01	Deciphered Date	2012/12/31

Compal Electronics, Inc.

Title: N13P-VGA CORE, GND

Size	Document Number	Rev
	Y490-LA8691P	0.2

Date: Tuesday, March 20, 2012 | Sheet 26 of 65



GDDR5
Mode H – Mirror Mode Mapping

Address	DATA Bus 0..31	32..63
FBx_CMD0	CS#	
FBx_CMD1	A3_BA3	
FBx_CMD2	A2_BA0	
FBx_CMD3	A4_BA2	
FBx_CMD4	A5_BA1	
FBx_CMD5	WE#	
FBx_CMD6	A7_A8	
FBx_CMD7	A6_A11	
FBx_CMD8	ABI#	
FBx_CMD9	A12_RFU	
FBx_CMD10	A0_A10	
FBx_CMD11	A1_A9	
FBx_CMD12	RAS#	
FBx_CMD13	RST#	
FBx_CMD14	CKE#	
FBx_CMD15	CAS#	
FBx_CMD16		CS#
FBx_CMD17		A3_BA3
FBx_CMD18		A2_BA0
FBx_CMD19		A4_BA2
FBx_CMD20		A5_BA1
FBx_CMD21		WE#
FBx_CMD22		A7_A8
FBx_CMD23		A6_A11
FBx_CMD24		ABI#
FBx_CMD25		A12_RFU
FBx_CMD26		A0_A10
FBx_CMD27		A1_A9
FBx_CMD28		RAS#
FBx_CMD29		RST#
FBx_CMD30		CKE#
FBx_CMD31		CAS#

Security Classification	Compal Secret Data		
Issued Date	2011/11/01	Deciphered Date	2012/12/31

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Compal Electronics, Inc.

Title: **N13P-MEM Interface**

Size: C | Document Number: **Y490-LA8691P** | Rev: 0.2

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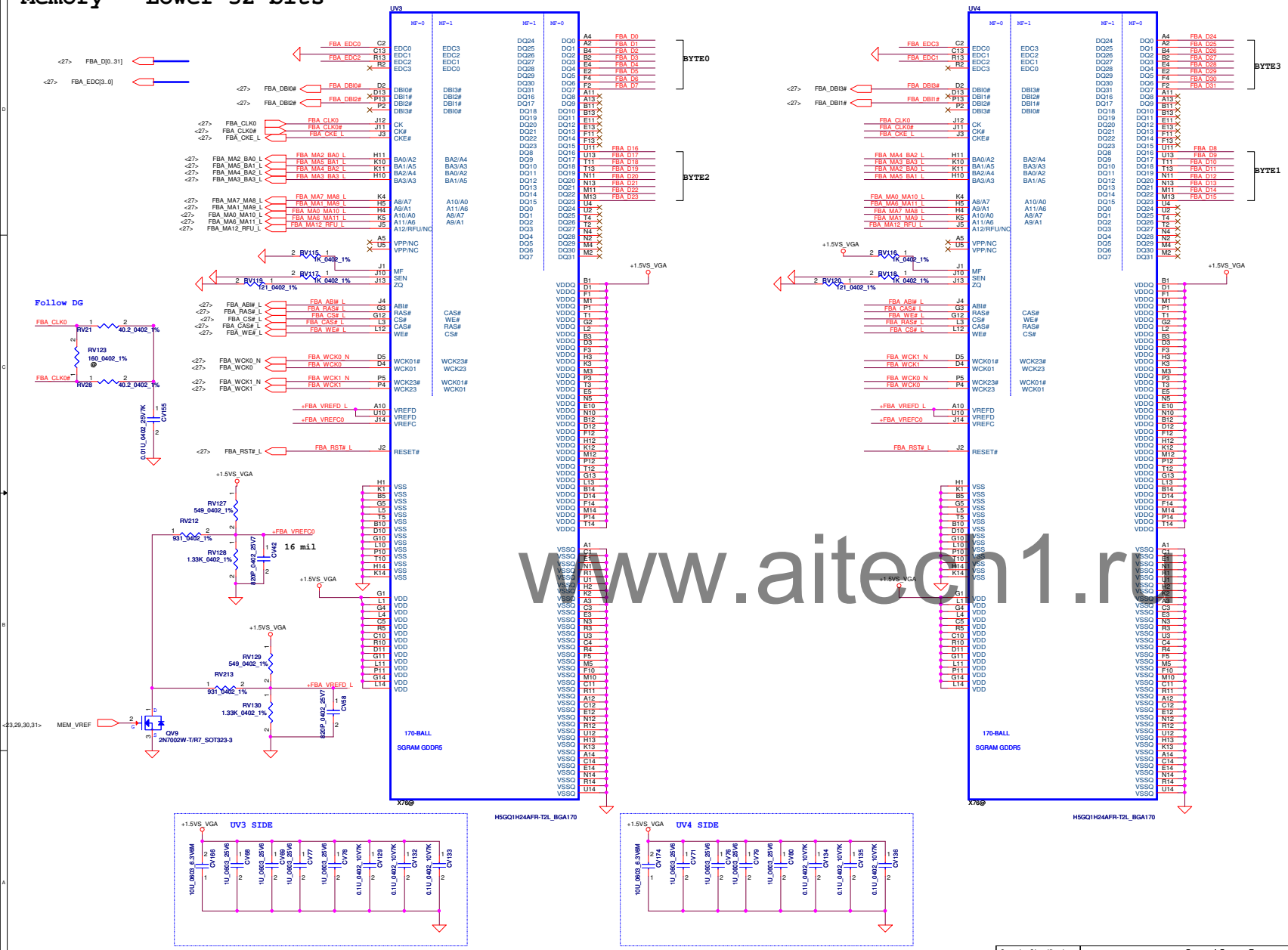
Memory - Lower 32 bits



GDDR5
Mode H - Mirror Mode Mapping

	DATA Bus	
Address	0..31	32..63
FBx_CMD0	CS#	
FBx_CMD1	A3_BA3	
FBx_CMD2	A2_BA0	
FBx_CMD3	A4_BA2	
FBx_CMD4	A5_BA1	
FBx_CMD5	WE#	
FBx_CMD6	A7_A8	
FBx_CMD7	A6_A11	
FBx_CMD8	ABI#	
FBx_CMD9	A12_RFU	
FBx_CMD10	A0_A10	
FBx_CMD11	A1_A9	
FBx_CMD12	RAS#	
FBx_CMD13	RST#	
FBx_CMD14	CKE#	
FBx_CMD15	CAS#	
FBx_CMD16		CS#
FBx_CMD17		A3_BA3
FBx_CMD18		A2_BA0
FBx_CMD19		A4_BA2
FBx_CMD20		A5_BA1
FBx_CMD21		WE#
FBx_CMD22		A7_A8
FBx_CMD23		A6_A11
FBx_CMD24		ABI#
FBx_CMD25		A12_RFU
FBx_CMD26		A0_A10
FBx_CMD27		A1_A9
FBx_CMD28		RAS#
FBx_CMD29		RST#
FBx_CMD30		CKE#
FBx_CMD31		CAS#

Security Classification	Compal Secret Data		
Issued Date	2011/11/01	Deciphered Date	2012/12/31

Compal Electronics, Inc.

Title: N13P-VRAM A Lower

Size | Document Number: Y490-LA8691P | Rev: 0.2

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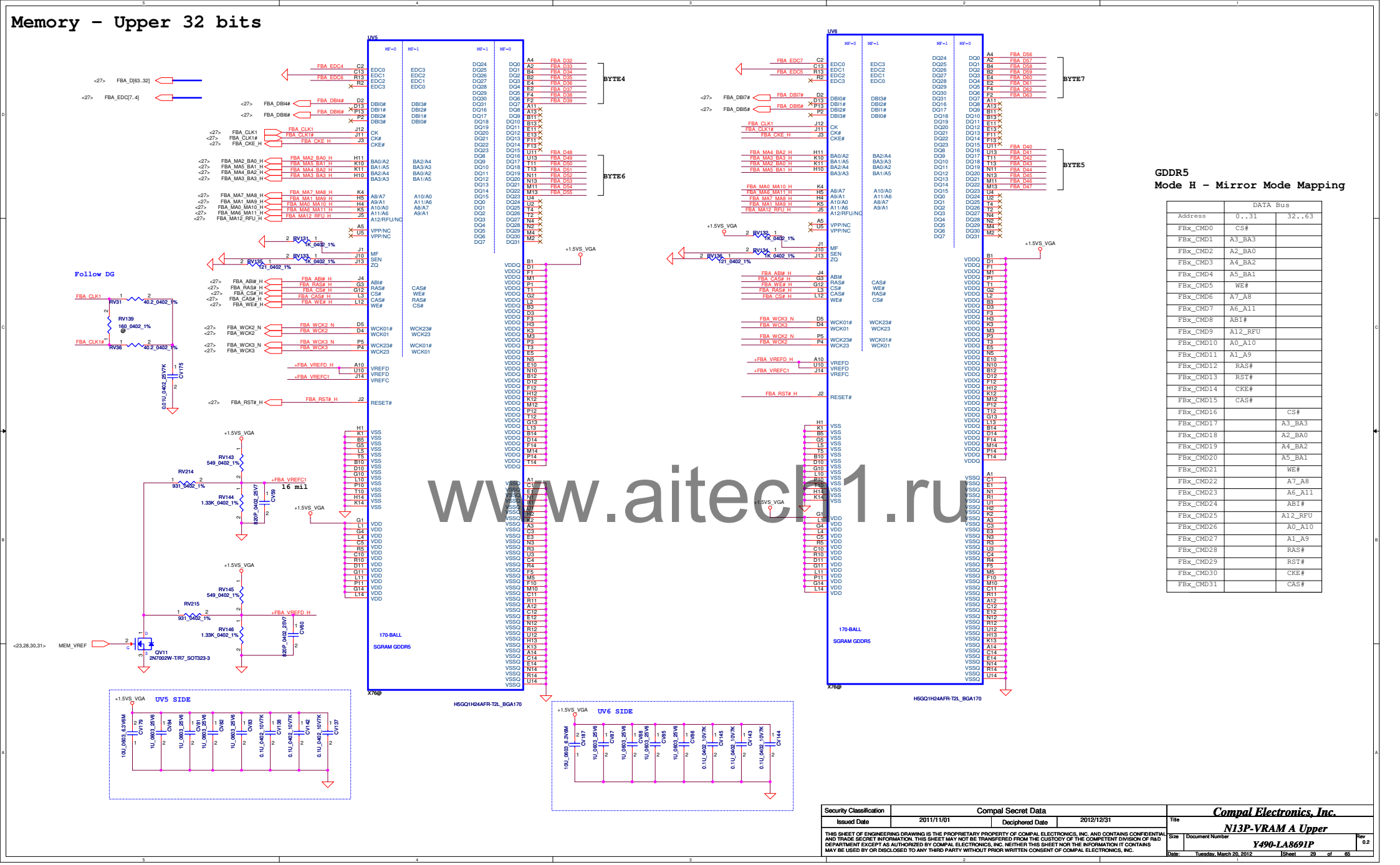
Memory - Upper 32 bits



GDDR5
Mode H - Mirror Mode Mapping

	DATA Bus	
Address	0..31	32..63
FBx_CMD0	CS#	
FBx_CMD1	A3_BA3	
FBx_CMD2	A2_BA0	
FBx_CMD3	A4_BA2	
FBx_CMD4	A5_BA1	
FBx_CMD5	WE#	
FBx_CMD6	A7_A8	
FBx_CMD7	A6_A11	
FBx_CMD8	ABI#	
FBx_CMD9	A12_RFU	
FBx_CMD10	A0_A10	
FBx_CMD11	A1_A9	
FBx_CMD12	RAS#	
FBx_CMD13	RST#	
FBx_CMD14	CKE#	
FBx_CMD15	CAS#	
FBx_CMD16		CS#
FBx_CMD17		A3_BA3
FBx_CMD18		A2_BA0
FBx_CMD19		A4_BA2
FBx_CMD20		A5_BA1
FBx_CMD21		WE#
FBx_CMD22		A7_A8
FBx_CMD23		A6_A11
FBx_CMD24		ABI#
FBx_CMD25		A12_RFU
FBx_CMD26		A0_A10
FBx_CMD27		A1_A9
FBx_CMD28		RAS#
FBx_CMD29		RST#
FBx_CMD30		CKE#
FBx_CMD31		CAS#

Security Classification	Compal Secret Data	
Issued Date	2011/11/01	Deciphered Date 2012/12/31

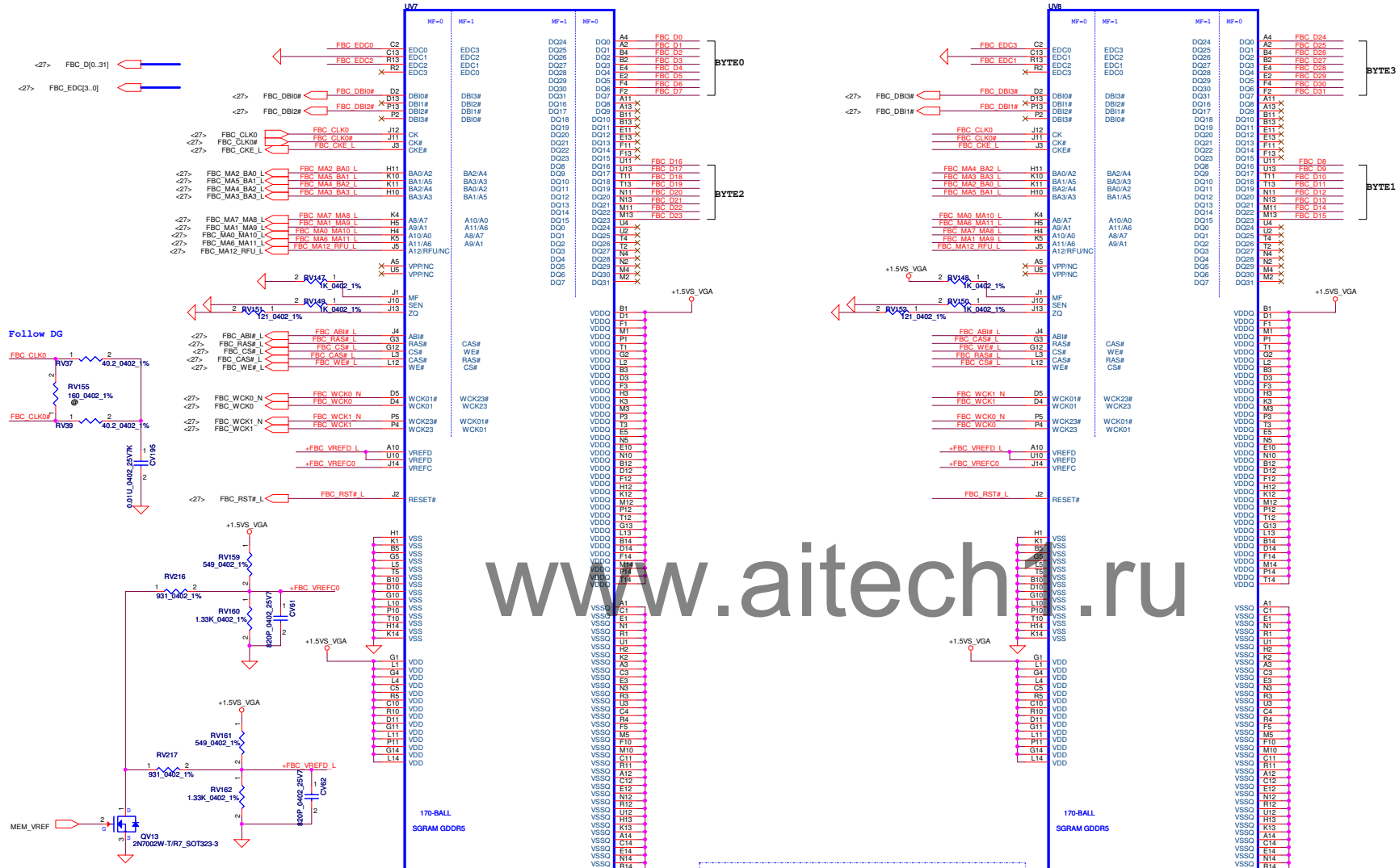
Compal Electronics, Inc.

Title: **N13P-VRAM A Upper**

Size: | Document Number: **Y490-LA8691P** | Rev: 0.2

Date: Tuesday, March 20, 2012 | Sheet 29 of 65

Memory Partition C – Lower 32 bits



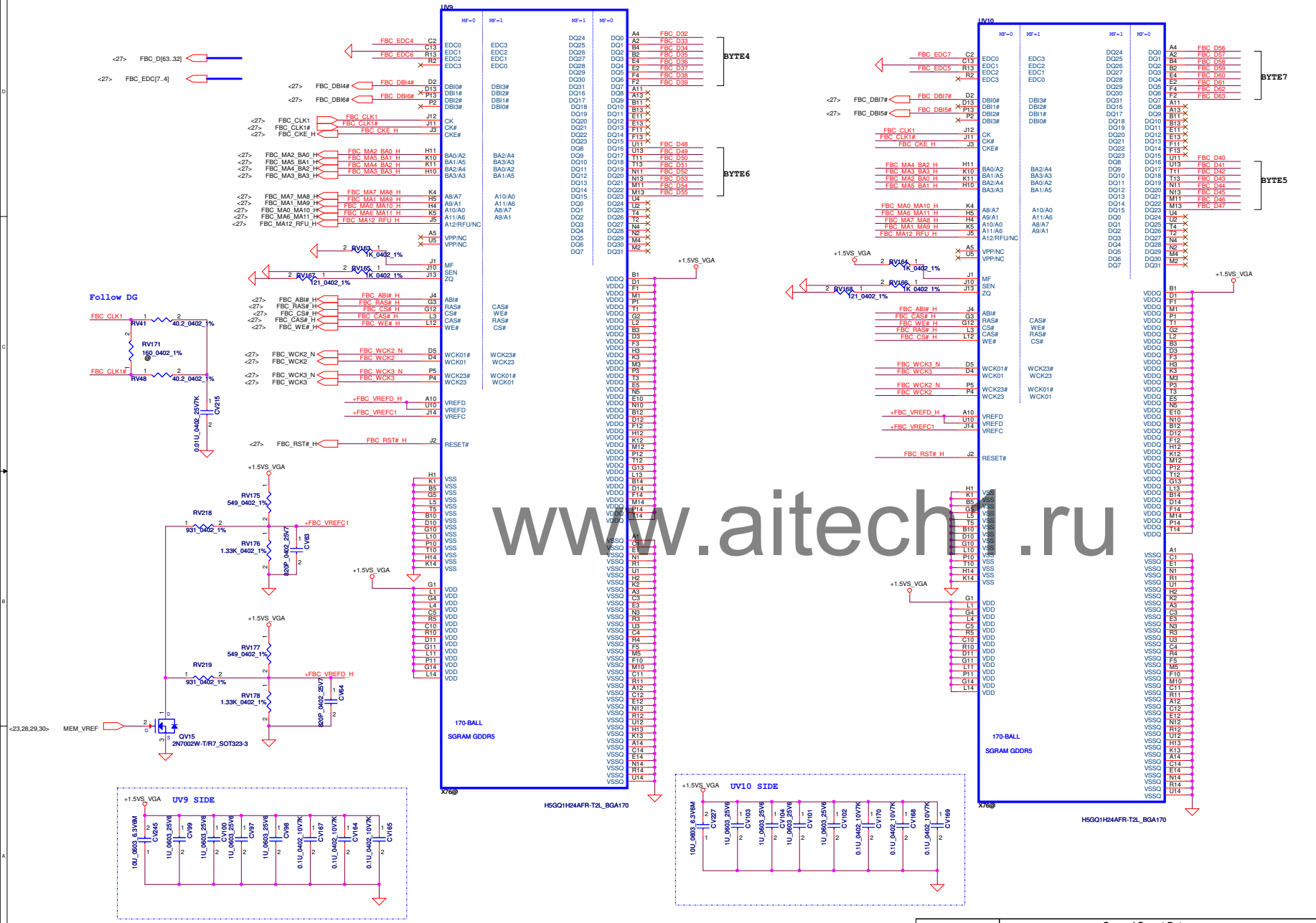
GDDR5
Mode H – Mirror Mode Mapping

	DATA Bus	
Address	0..31	32..63
FBx_CMD0	CS#	
FBx_CMD1	A3_BA3	
FBx_CMD2	A2_BA0	
FBx_CMD3	A4_BA2	
FBx_CMD4	A5_BA1	
FBx_CMD5	WE#	
FBx_CMD6	A7_A8	
FBx_CMD7	A6_A11	
FBx_CMD8	ABI#	
FBx_CMD9	A12_RFU	
FBx_CMD10	A0_A10	
FBx_CMD11	A1_A9	
FBx_CMD12	RAS#	
FBx_CMD13	RST#	
FBx_CMD14	CKE#	
FBx_CMD15	CAS#	
FBx_CMD16		CS#
FBx_CMD17		A3_BA3
FBx_CMD18		A2_BA0
FBx_CMD19		A4_BA2
FBx_CMD20		A5_BA1
FBx_CMD21		WE#
FBx_CMD22		A7_A8
FBx_CMD23		A6_A11
FBx_CMD24		ABI#
FBx_CMD25		A12_RFU
FBx_CMD26		A0_A10
FBx_CMD27		A1_A9
FBx_CMD28		RAS#
FBx_CMD29		RST#
FBx_CMD30		CKE#
FBx_CMD31		CAS#

Security Classification	Compal Secret Data		
Issued Date	2011/11/01	Deciphered Date	2011/12

Compal Electronics, Inc.			
Title	N12P-VRAM C Lower		
Size	Document Number		Rev
B	Y490-LA8691P		0.2
Date:	Tuesday, March 20, 2012	Sheet	30 of 65

Memory Partition C – Upper 32 bits

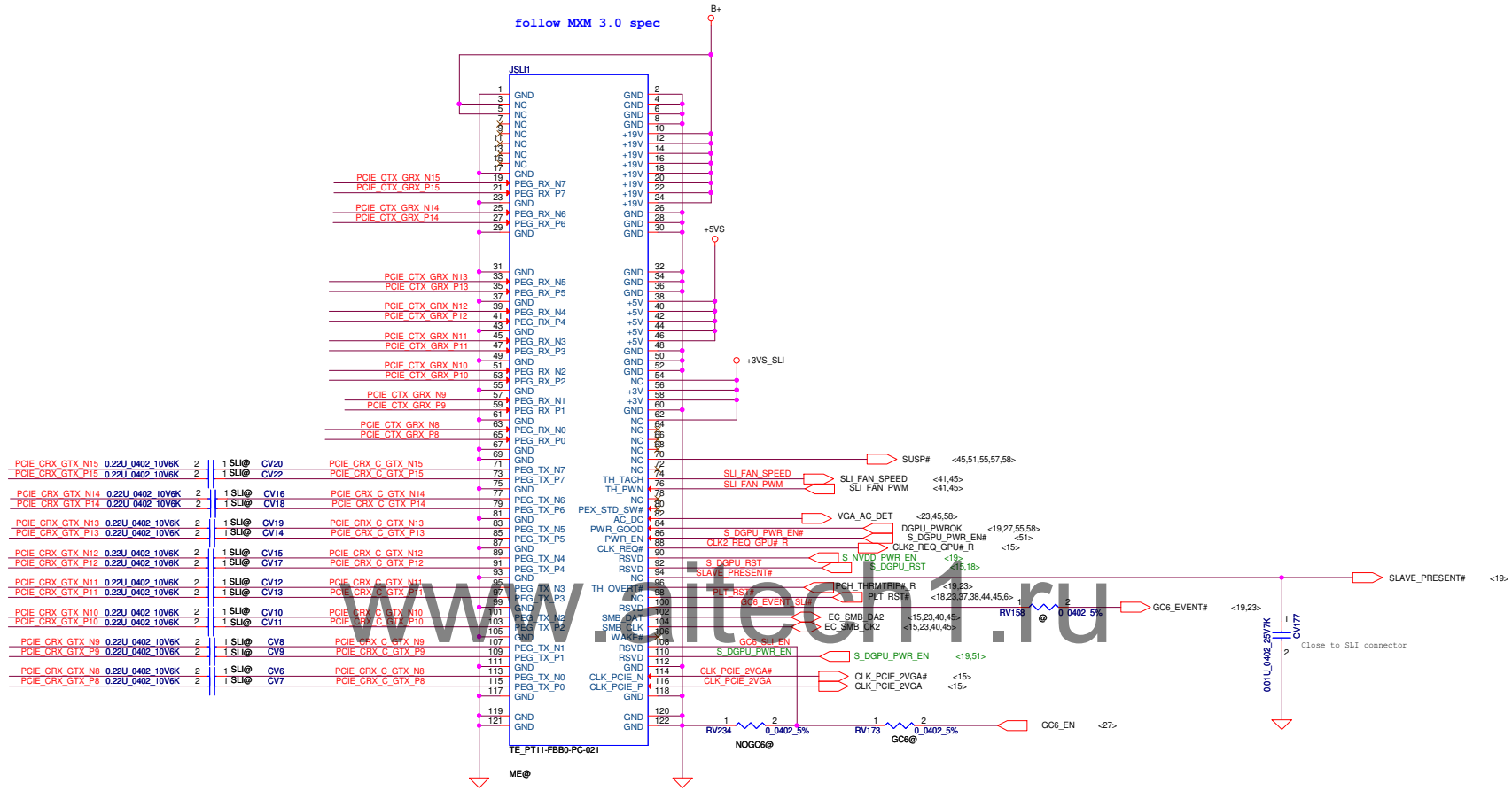


GDDR5
Mode H – Mirror Mode Mapping

	DATA Bus	
Address	0..31	32..63
FBx_CMD0	CS#	
FBx_CMD1	A3_BA3	
FBx_CMD2	A2_BA0	
FBx_CMD3	A4_BA2	
FBx_CMD4	A5_BA1	
FBx_CMD5	WE#	
FBx_CMD6	A7_A8	
FBx_CMD7	A6_A11	
FBx_CMD8	ABI#	
FBx_CMD9	A12_RFU	
FBx_CMD10	A0_A10	
FBx_CMD11	A1_A9	
FBx_CMD12	RAS#	
FBx_CMD13	RST#	
FBx_CMD14	CKE#	
FBx_CMD15	CAS#	
FBx_CMD16		CS#
FBx_CMD17		A3_BA3
FBx_CMD18		A2_BA0
FBx_CMD19		A4_BA2
FBx_CMD20		A5_BA1
FBx_CMD21		WE#
FBx_CMD22		A7_A8
FBx_CMD23		A6_A11
FBx_CMD24		ABI#
FBx_CMD25		A12_RFU
FBx_CMD26		A0_A10
FBx_CMD27		A1_A9
FBx_CMD28		RAS#
FBx_CMD29		RST#
FBx_CMD30		CKE#
FBx_CMD31		CAS#

Security Classification	Compal Secret Data		
Issued Date	2011/11/01	Deciphered Date	2011/12

Compal Electronics, Inc.			
Title	N12P-VRAM C Upper		
Size	Document Number	Rev	
B	Y490-LA8691P	0.2	
Date: Tuesday, March 20, 2012	Sheet 31 of 65		



11/11 for 2nd VGA fan need to notic EC

<23,5> PCIE_CTX_GRX_N[0..15] PCIE_CTX_GRX_N[0..15]
<23,5> PCIE_CTX_GRX_P[0..15] PCIE_CTX_GRX_P[0..15]
<23,5> PCIE_CRX_GTX_N[0..15] PCIE_CRX_GTX_N[0..15]
<23,5> PCIE_CRX_GTX_P[0..15] PCIE_CRX_GTX_P[0..15]

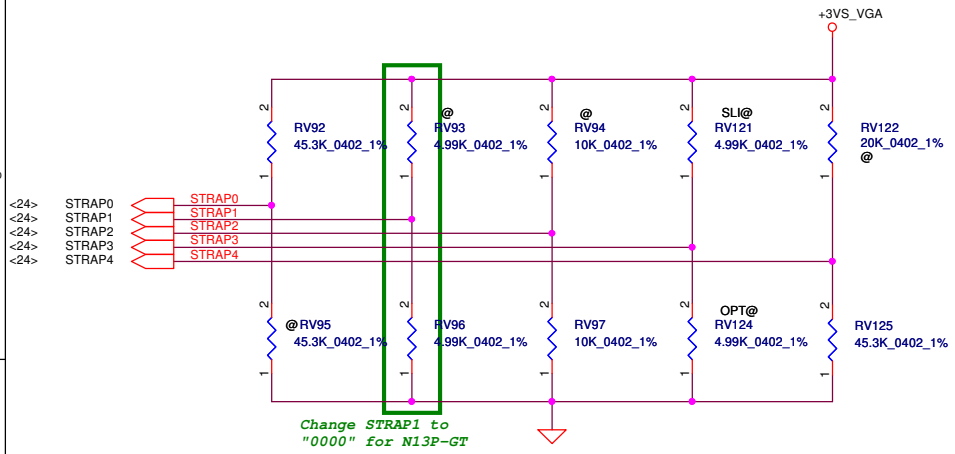
Security Classification	Compal Secret Data		
Issued Date	2011/11/01	Deciphered Date	2012/12/31

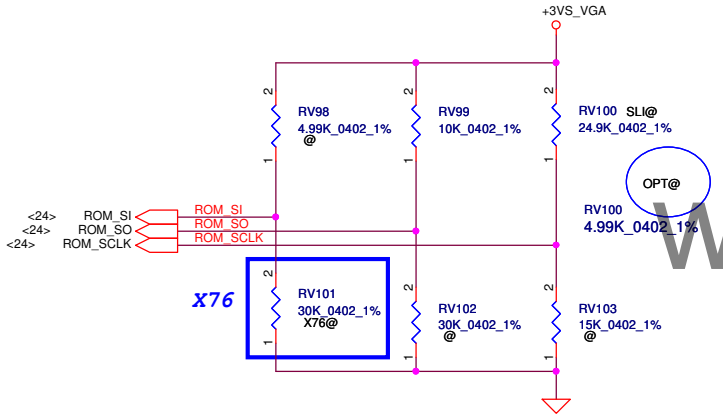
Compal Electronics, Inc.

Title: **DDRIII-SODIMM SLOT1**

Size: Custom | Document Number: **Y490-LA8691P** | Rev: 0.2

Date: Tuesday, March 20, 2012 | Sheet 32 of 65





Physical Strapping pin	Power Rail	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SCLK	+3VS_VGA	PCI_DEVID[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLL_EN_TERM
ROM_SI	+3VS_VGA	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SO	+3VS_VGA	FB[1]	FB[0]	SMB_ALT_ADDR	VGA_DEVICE
STRAP0	+3VS_VGA	USER[3]	USER[2]	USER[1]	USER[0]
STRAP1	+3VS_VGA	3GIO_PAD_CFG_ADR[3]	3GIO_PAD_CFG_ADR[2]	3GIO_PAD_CFG_ADR[1]	3GIO_PAD_CFG_ADR[0]
STRAP2	+3VS_VGA	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
STRAP3	+3VS_VGA	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
STRAP4	+3VS_VGA	RESERVED	PCIE_SPEED_CHANGE_GEN3	PCIE_MAX_SPEED	DP_PLL_VDD33V

Resistor Values	Pull-up to +3VS_VGA	Pull-down to Gnd
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111

SLOT_CLK_CFG	
0	GPU and MCH don't share a common reference clock
1	GPU and MCH share a common reference clock (Default)

SUB_VENDOR	
0	No VBIOS ROM (Default)
1	BIOS ROM is present

3GIO_PADCFG	
3GIO_PADCFG[3:0]	
0000	Notebook Default

XCLK_417	
0	277MHz (Default)
1	Reserved

USER Straps	
User[3:0]	
1000-1100	Customer defined

PEX_PLL_EN_TERM	
0	Disable (Default)
1	Enable

PCIE_MAX_SPEED	
0	Limit to PCIE Gen1
1	PCIE Gen 2/3 Capable

FB_0_BAR_SIZE	
0	Reserved
1	Reserved
2	256MB (Default)
3	Reserved

SMBUS_ALT_ADDR	
0	0x9E (Default)
1	0x9C (Multi-GPU usage)

VGA_DEVICE	
0	3D Device (Class Code 302h)
1	VGA Device (Default)

X76

GPU	FB Memory (GDDR5)		ROM_SI	ROM_SO	ROM_SCLK	STRAP0	STRAP1	STRAP2	STRAP3	STRAP4
N13P-GT1 28nm	Samsung	K4G20325FD-FC04 2G 64Mx32	PD 30K	PU 10K	PU 25K (SLI) PU 5K (OPT)	PU 45K	PD 5K	PD 10K	PU 5K	PD 10K
		K4G10325FG-HC04 1G 32Mx32	PD 45K							
	Hynix	H5GQ2H24MFR-T2C 2G 64Mx32	PD 25K							
		H5GQ1H24BFR-T2C 1G 32Mx32	PD 35K							

VRAM	X76	VRAM P/N
Samsung	X76409JVL01 (2G 64Mx32)	SA00005B70J
Hynix	X76409JVL02 (2G 64Mx32)	SA00004GD0J

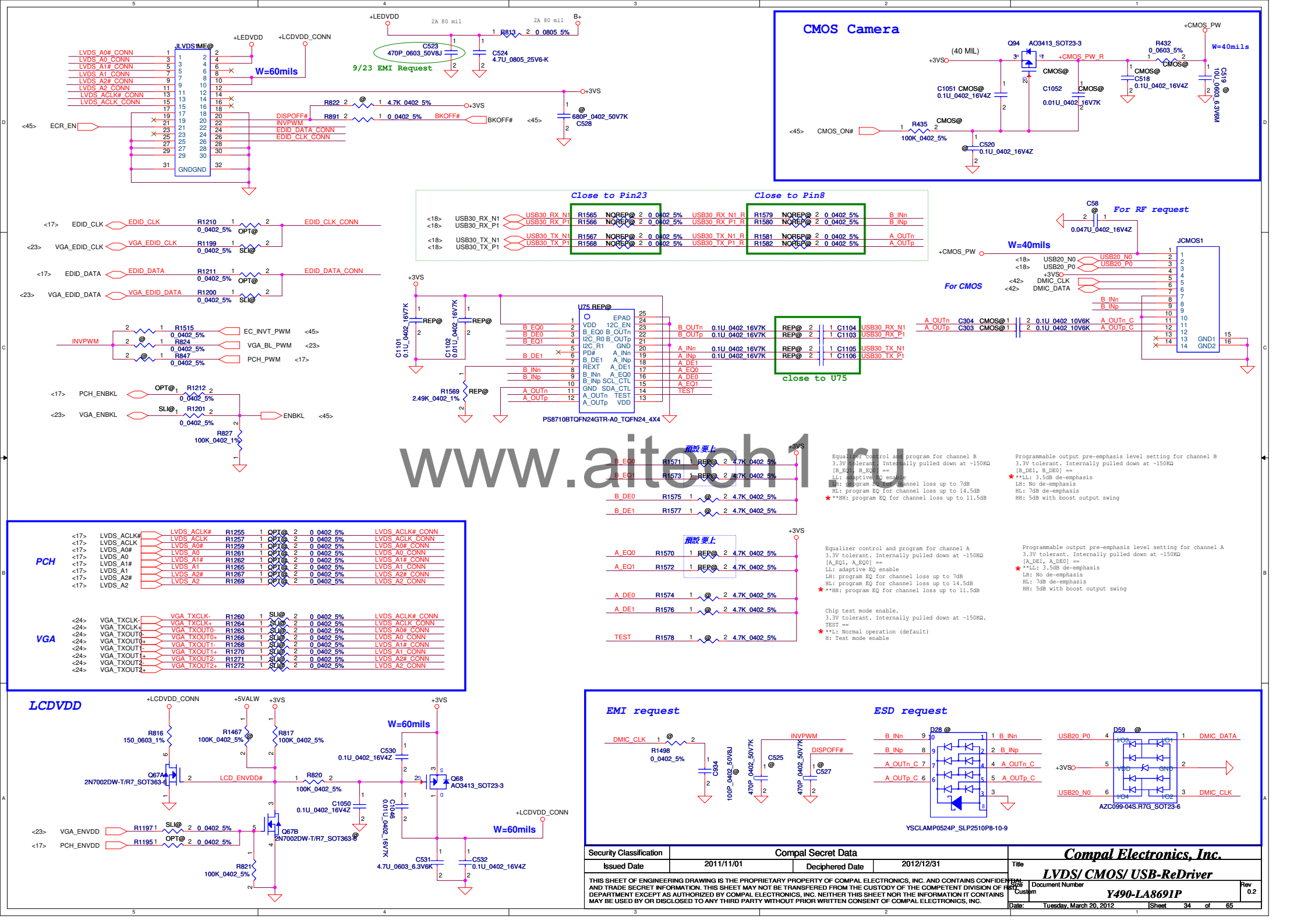
Security Classification	Compal Secret Data		
Issued Date	2011/11/01	Deciphered Date	2012/12/31

Compal Electronics, Inc.

Title: N13P_MISC

Size: Custom | Document Number: Y490-LA8691P | Rev: 0.2

Date: Tuesday, March 20, 2012 | Sheet 33 of 65



Security Classification	Compal Secret Data		
Issued Date	2011/11/01	Deciphered Date	2012/12/31

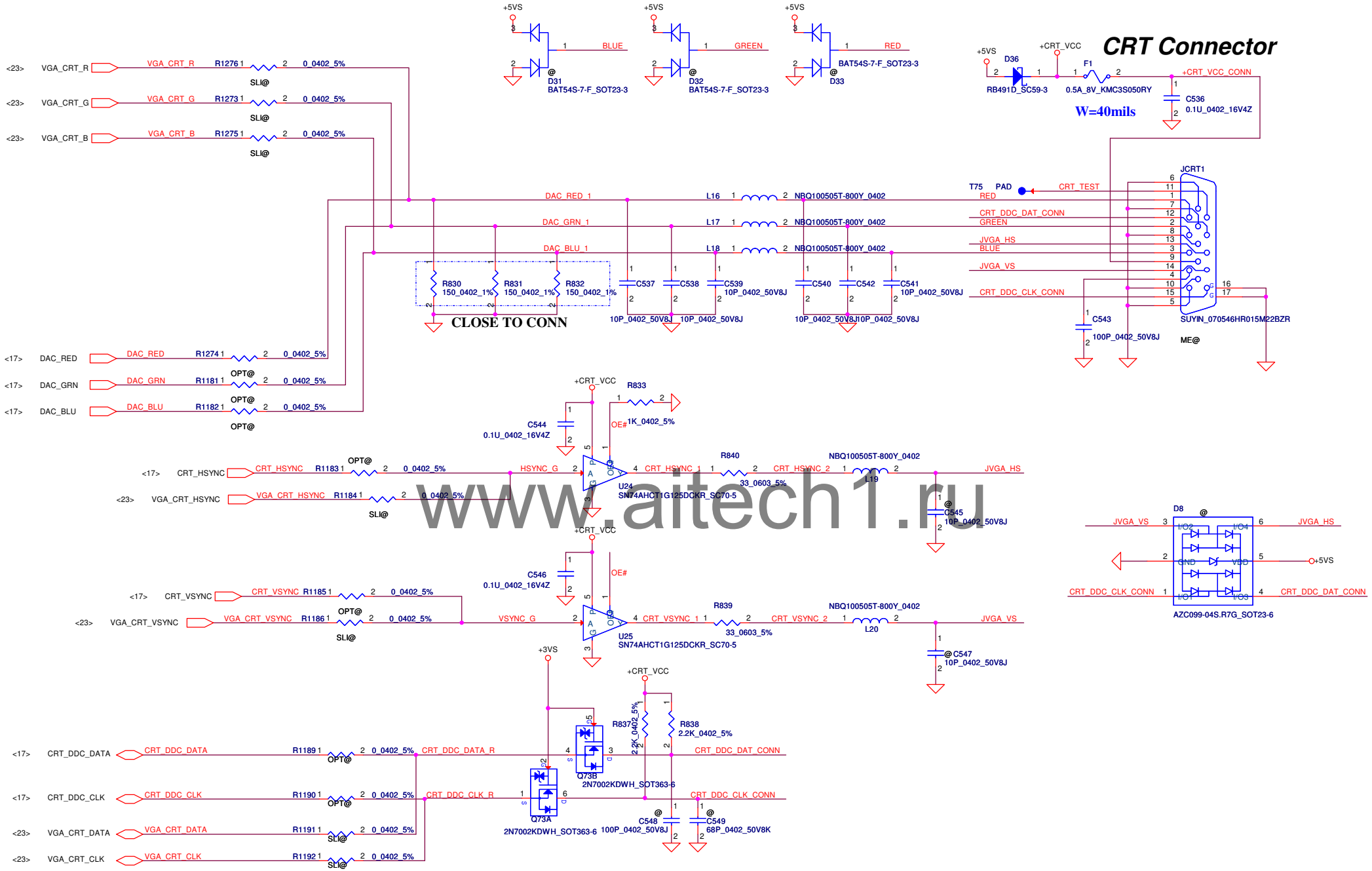
Compal Electronics, Inc.

Title: **LVDS/ CMOS/ USB-ReDriver**

Size	Document Number	Rev
Custom	Y490-LA8691P	0.2

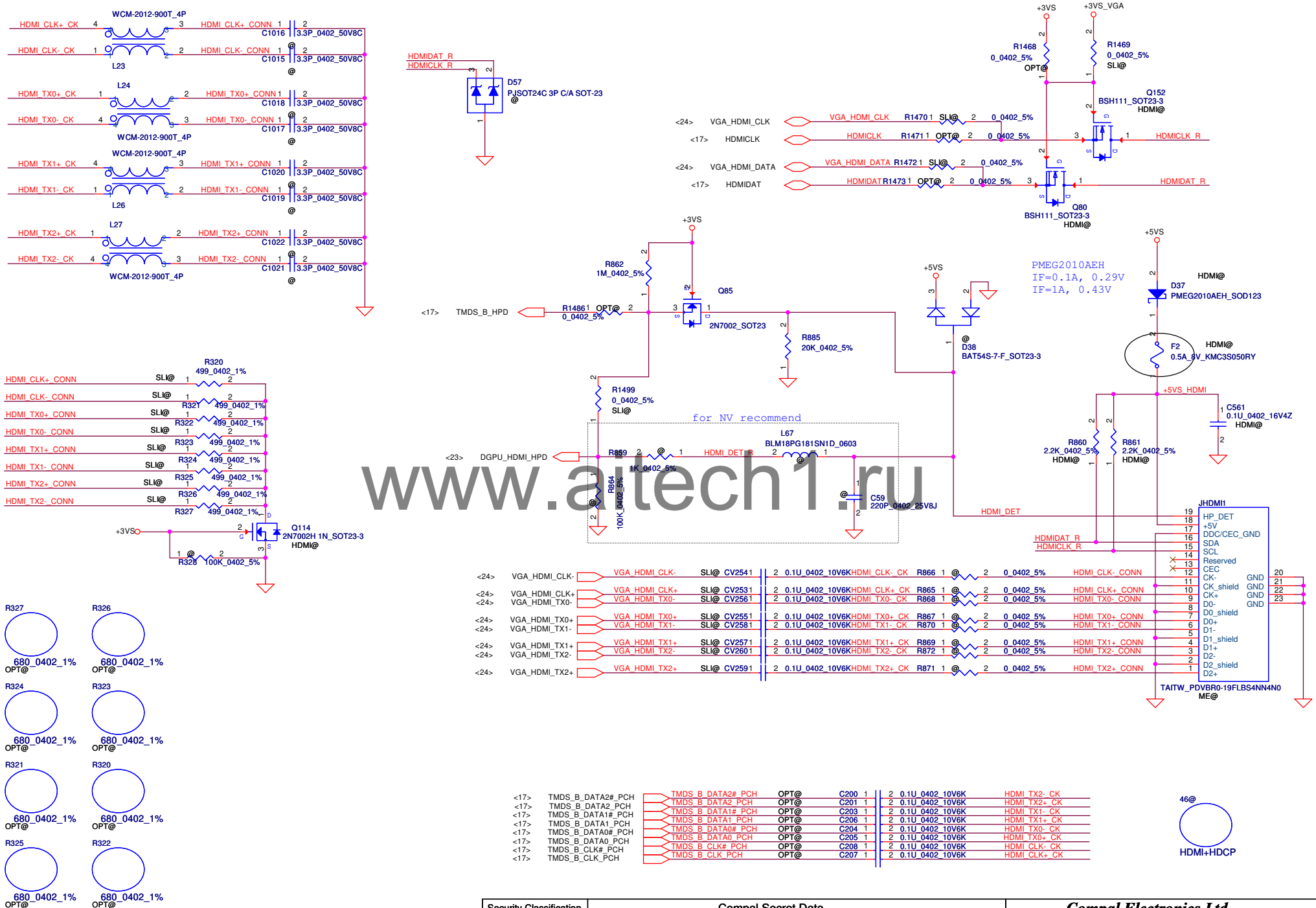
Date: Tuesday, March 20, 2012 Sheet 34 of 65

CRT Connector



Security Classification	Compal Secret Data		
Issued Date	2011/11/01	Deciphered Date	2012/12/31

Compal Electronics, Inc.			
Title: CRT Connector			
Size: Custom	Document Number: Y490-LA8691P		Rev: 0.2
Date: Tuesday, March 20, 2012	Sheet 35 of 65		



Security Classification	Compal Secret Data		
Issued Date	2011/11/01	Deciphered Date	2012/12/31

Compal Electronics,Ltd.

Title: **HDMI CONN**

Size	Document Number	Rev
Custom	Y490-LA8691P	0.2

Date: Tuesday, March 20, 2012 | Sheet 36 of 65

Mini-Express Card for WLAN/WiMAX(Half)
Mini-Express Card for SSD(Full)

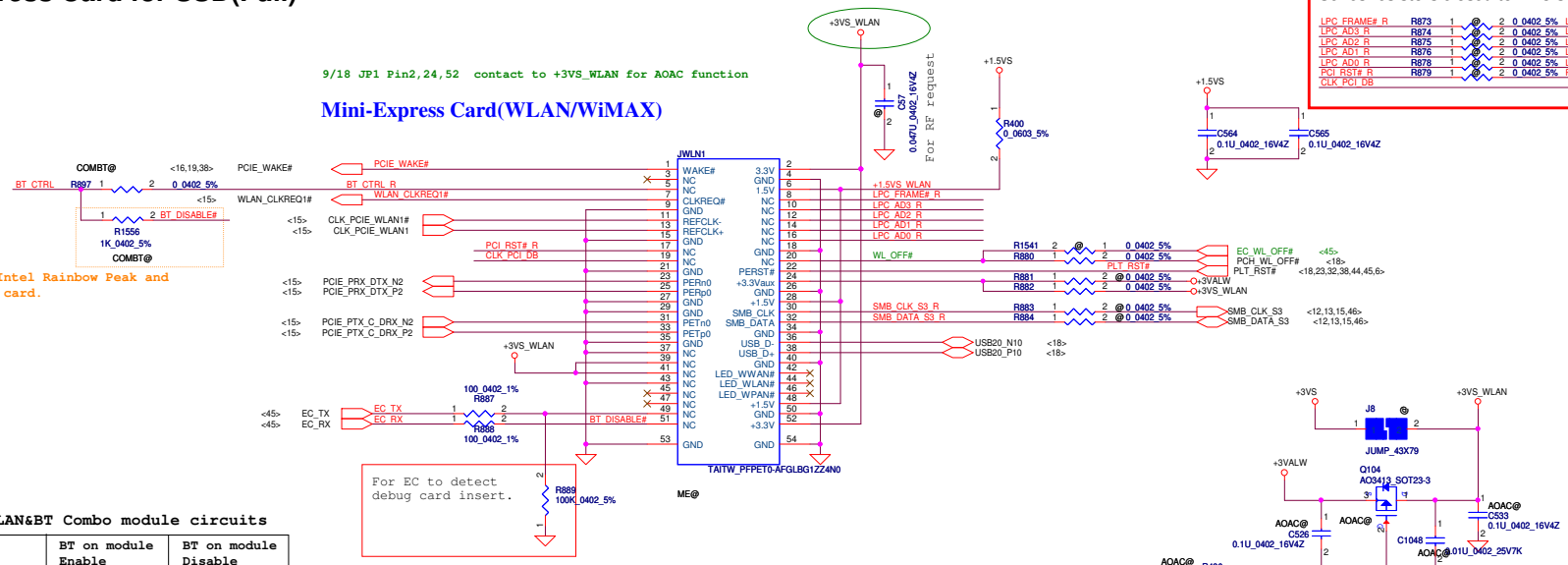
Reserve for SW mini-pcie debug card.
Series resistors closed to KBC side.

LPC_FRAME# R	R873	1	@	2	0_0402_5%	LPC_FRAME#
LPC_AD3 R	R874	1	@	2	0_0402_5%	LPC_AD3
LPC_AD2 R	R875	1	@	2	0_0402_5%	LPC_AD2
LPC_AD1 R	R876	1	@	2	0_0402_5%	LPC_AD1
LPC_AD0 R	R878	1	@	2	0_0402_5%	LPC_AD0
PCI_RST# R	R879	1	@	2	0_0402_5%	PLT_RST#
CLK_PCI_DB						CLK_PCI_DB

LPC_FRAME# <14,45>
LPC_AD3 <14,45>
LPC_AD2 <14,45>
LPC_AD1 <14,45>
LPC_AD0 <14,45>
CLK_PCI_DB <18>

9/18 JP1 Pin2,24,52 contact to +3VS_WLAN for AOAC function

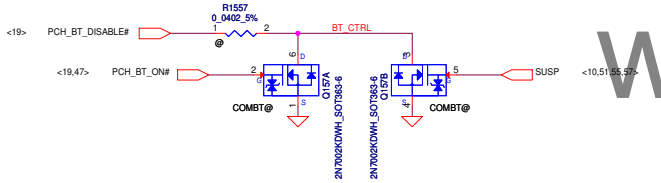
Mini-Express Card(WLAN/WiMAX)



For isolate Intel Rainbow Peak and Compal debug card.

WLAN&BT Combo module circuits

	BT on module Enable	BT on module Disable
BT_CRTL	H	L
PCH_BT_ON#	L	H

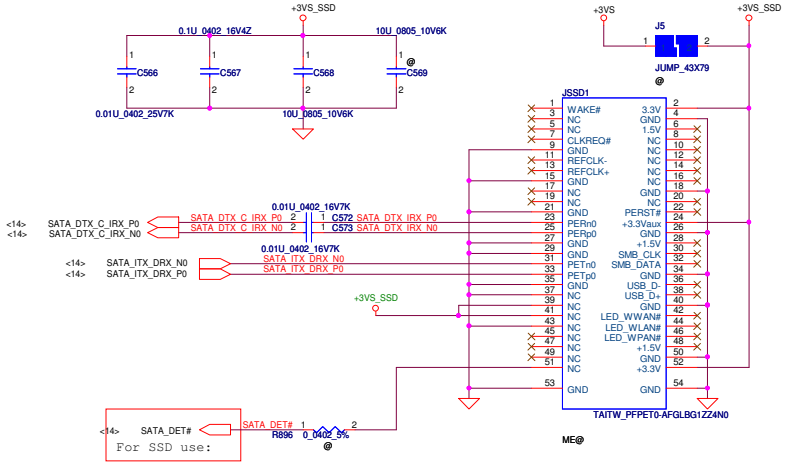


softstart (RC) will check on EVT PCB

9/18 Increase for Intel AOAC function

Mini-Express Card(SSD)

SSD Active:4.5W(1.5A)



Security Classification	Compal Secret Data		
Issued Date	2011/11/01	Deciphered Date	2012/12/31

Compal Electronics, Inc.			
Title: Mini-Card			
Size	Document Number: Y490-LA8691P		Rev: 0.2
Date: Tuesday, March 20, 2012		Sheet 37 of 65	

Atheros request can't disable LAN power

Layout Notice : Place as close chip as possible.

Vendor recommand reseve the PU resistor close LAN chip

	LX Voltage <Pin 40>	Configure
AR8151	+1.7V <VDDCT>	R1356,C955
AR8161	+1.1V <DVDDL,AVDDL>	R1357,R1372,L76

Close together

Note: Place Close to LAN chip
L39 DCR< 0.15 ohm
Rate current > 1A

Close to Pin40

Place close to Pin34

Place Close to Chip

H --> Overclocking mode
L --> Not overclocking mode

2011103 for vendor comment

Place Close to PIN1

Place Close to PIN10

Place Close to LAN chip

Note : C938, C940, C942, 944, reserved for EMI.

For AR8151: Stuff 49.9K and 0.1u
For AR8161: NC

For AR8151: Stuff C966,R1366
For AR8161: NC

Near Pin13 Near Pin19 Near Pin31 Near Pin6 Near Pin9 Near Pin22 Near Pin37 Near Pin24

Place close to Pin16

For AR8151: Stuff R1368 for +AVDD3.3
For AR8161: Stuff R1367,C949 for +AVDDH

Change C968, C969 value of Cap from 33pF to 15pF for TXC recommend

Security Classification	Compal Secret Data		
Issued Date	2011/11/01	Deciphered Date	2012/12/31

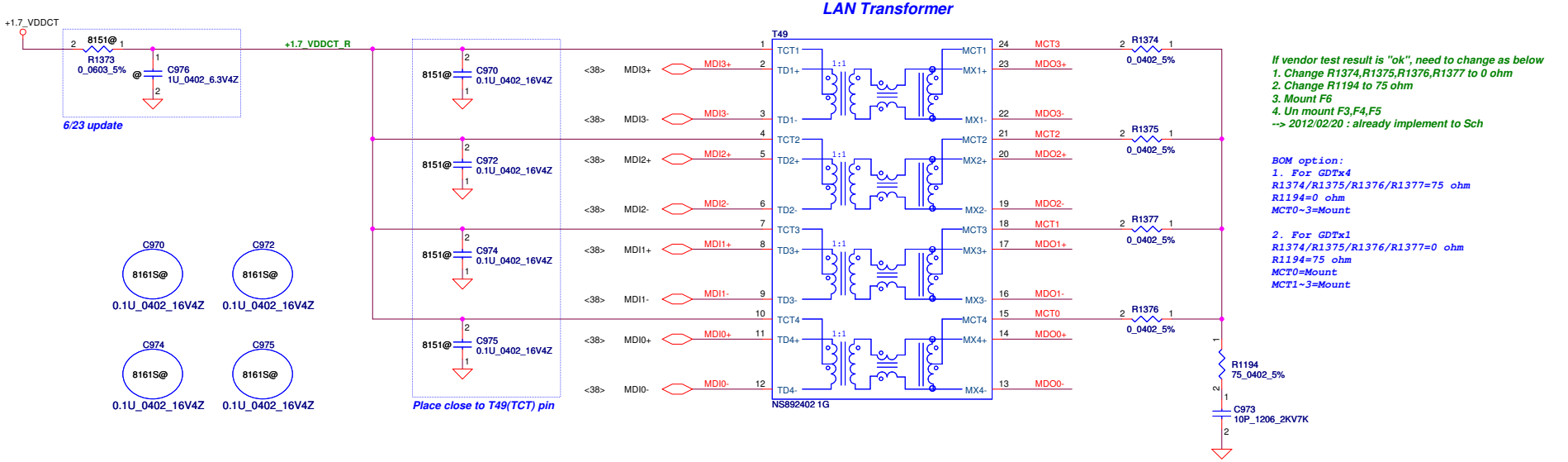
Compal Electronics, Inc.

Title: LAN-AR8151/8161

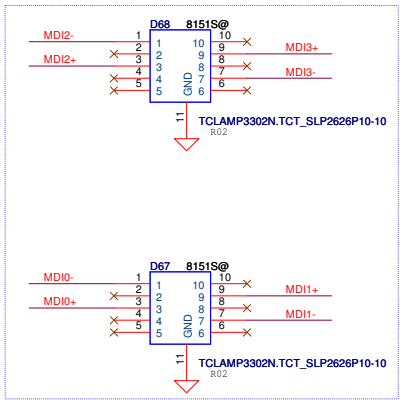
Size: Custom | Document Number: Y490-LA8691P | Rev: 0.2

Date: Tuesday, March 20, 2012 | Sheet 38 of 65

LAN Transformer

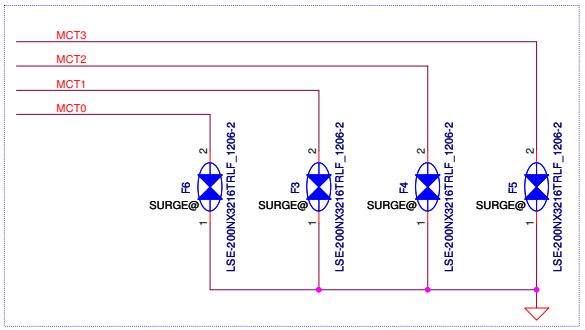


Place Close to T49



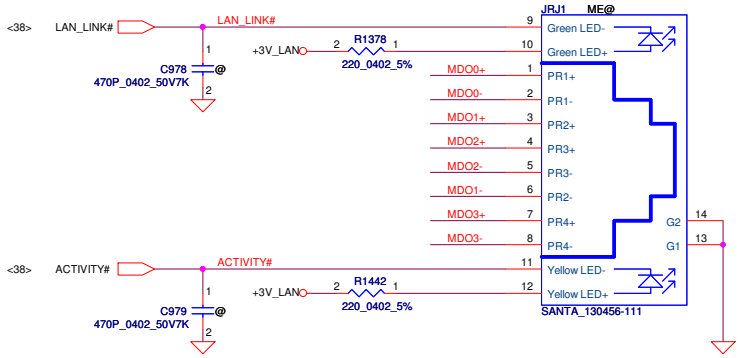
Reserve D67,D68 for EMI go rural solution

Place Close to T49



Reserve for EMI go rural solution

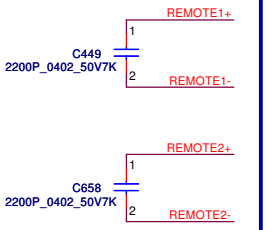
LAN Conn.



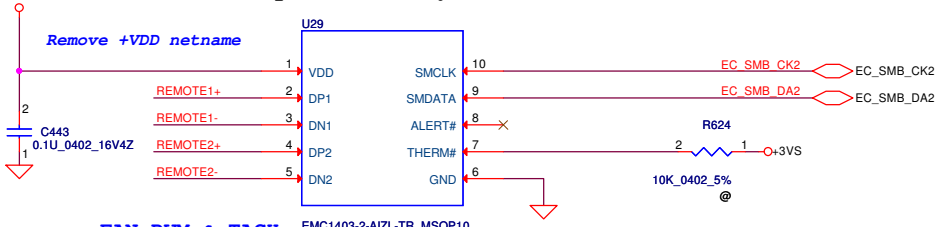
Security Classification	Compal Secret Data		
Issued Date	2011/11/01	Deciphered Date	2012/12/31

Compal Electronics, Inc.			
Title	LAN Transformer		
Size: Custom	Document Number: Y490-LA8691P		Rev: 0.2
Date: Tuesday, March 20, 2012	Sheet 39 of 65		

Close U29



SMSC thermal sensor placed near by VRAM

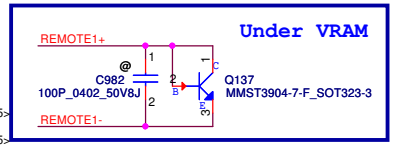


FAN_PWM & TACH for PWM FAN

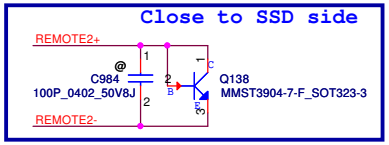
Address 1001_101xb

internal pull up 1.2K to 1.5V
R for initial thermal shutdown temp

Under VRAM

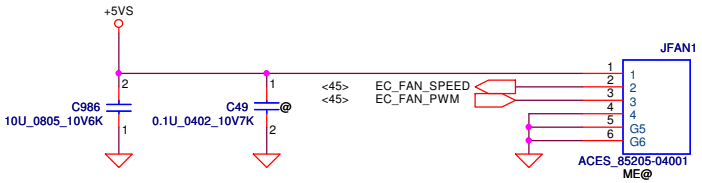


Close to SSD side



REMOTE2+/-:
Trace width/space:10/10 mil
Trace length:<8"

FAN1 Conn



Security Classification	Compal Secret Data		
Issued Date	2011/11/01	Deciphered Date	2012/12/31

Compal Electronics,Ltd.

Title: EMC1403/2103_Thermal sensor/FAN

Size	Document Number	Rev
Custom	Y490-LA8691P	0.2

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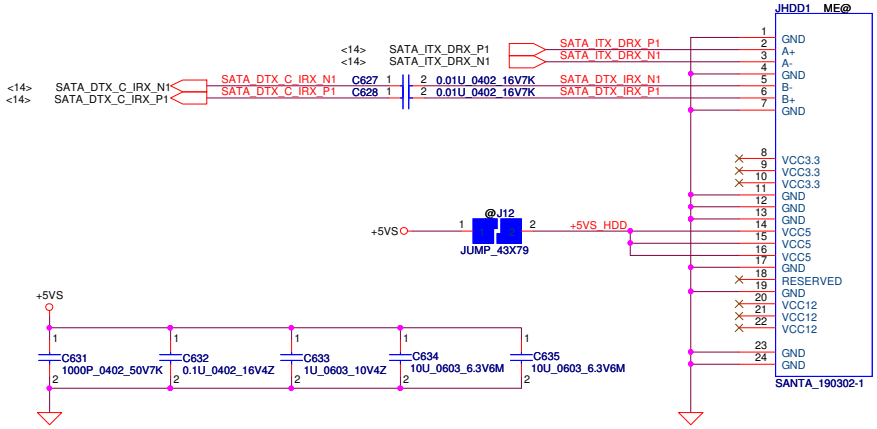
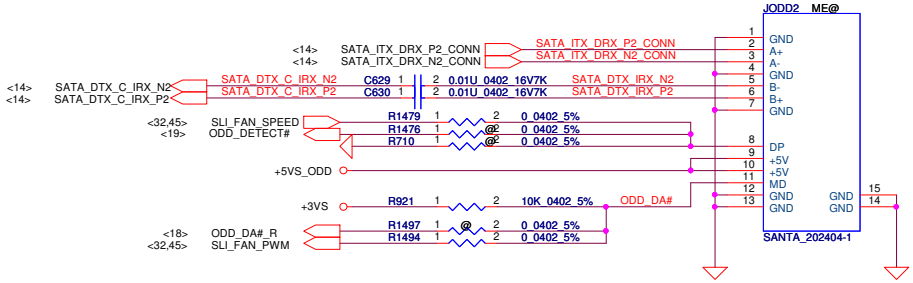
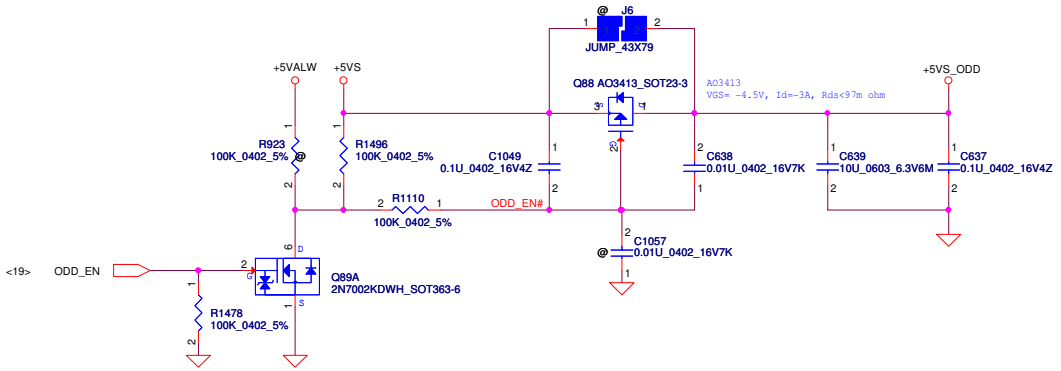
SATA HDD Conn.

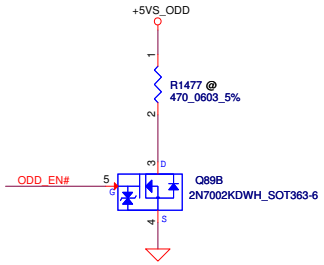


SATA ODD Conn.



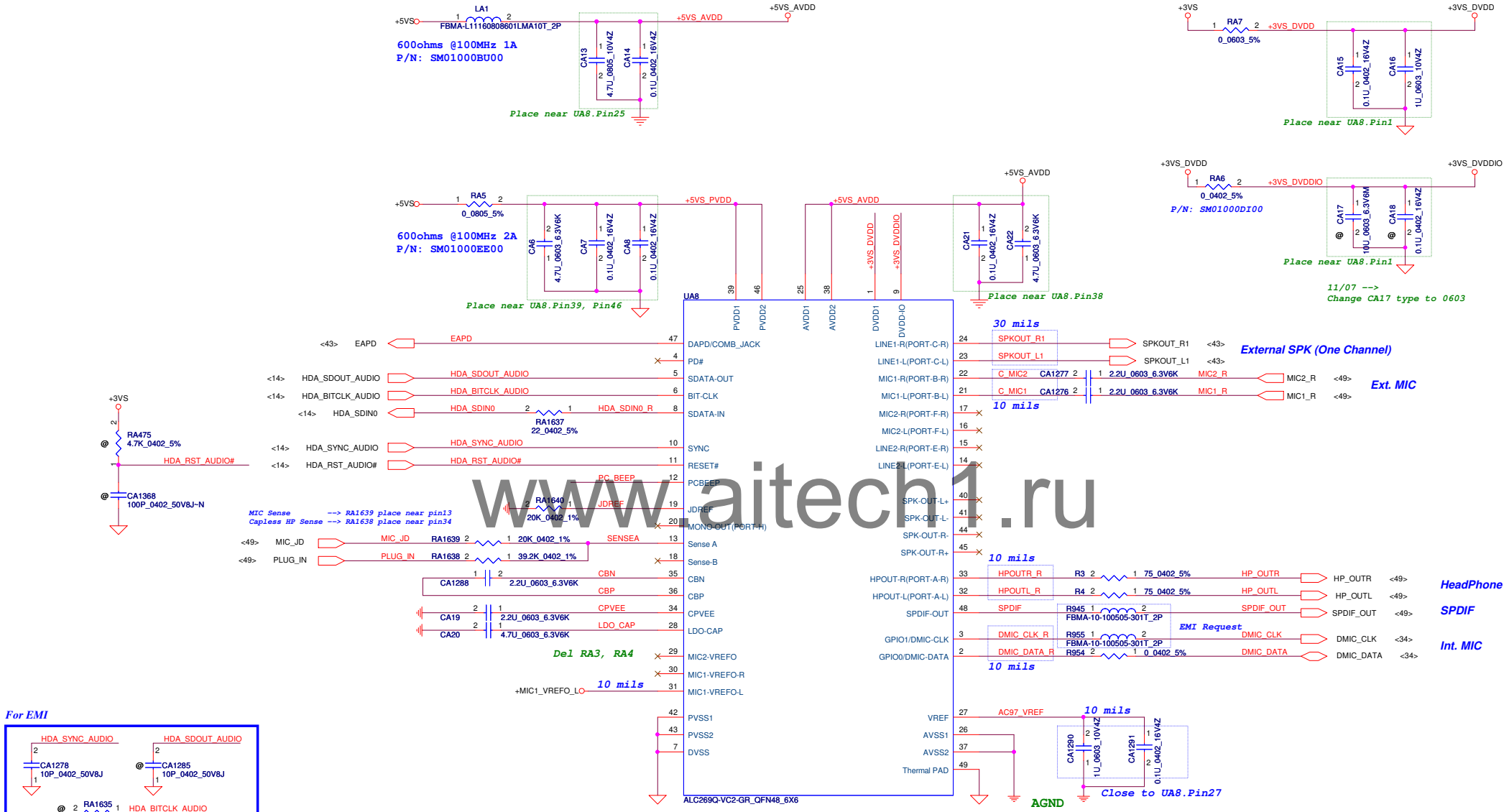
ODD Power Control





Security Classification	Compal Secret Data		
Issued Date	2011/11/01	Deciphered Date	2012/12/31

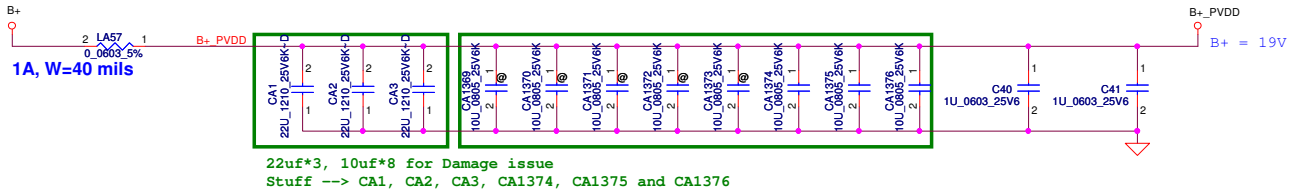
Compal Electronics, Inc.			
Title: HDD/ODD Connector			
Size: Custom	Document Number: Y490-LA8691P		Rev: 0.2
Date: Tuesday, March 20, 2012	Sheet 41 of 65		



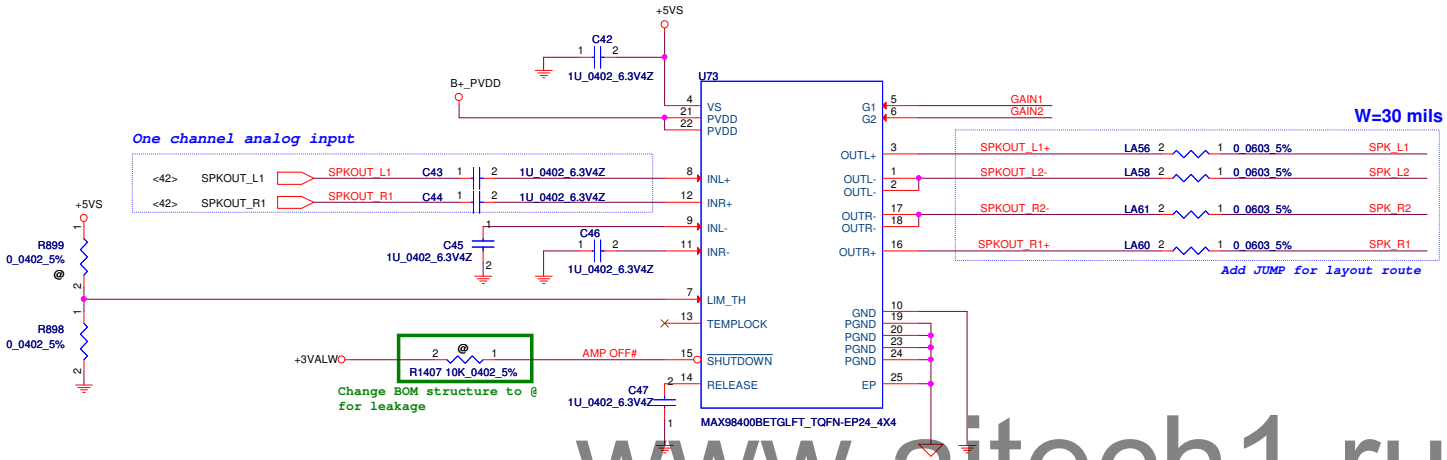
Pin Assignment	Location	Function
SPK-OUT (Pin40/41/44/45)	Internal	Int Speaker
Capless HP-OUT (Pin32/33)	External	Headphone out
MIC1(Pin21/22)	External	Mic in

Security Classification	Compal Secret Data		
Issued Date	2011/11/01	Deciphered Date	2012/03/09

Compal Electronics, Inc.			
Title: HD Audio ALC269Q-VC3			
Size: Custom	Document Number: Y490-LA8691P		Rev: 0.2
Date: Tuesday, March 20, 2012	Sheet 42 of 65		



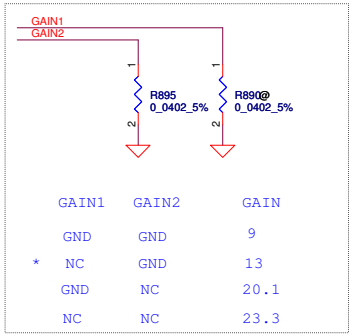
22uf*3, 10uf*8 for Damage issue
Stuff --> CA1, CA2, CA3, CA1374, CA1375 and CA1376



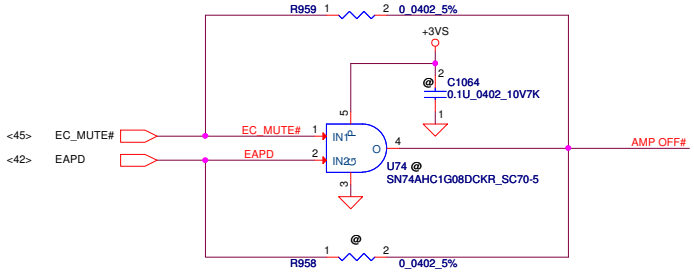
W=30 mils

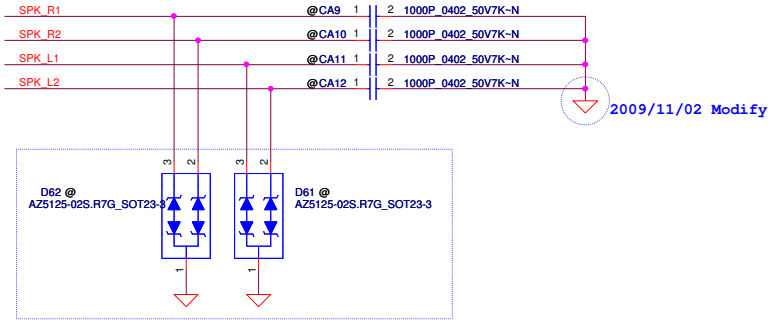
Add JUMP for layout route

GAIN SETTING



	GAIN1	GAIN2	GAIN
	GND	GND	9
*	NC	GND	13
	GND	NC	20.1
	NC	NC	23.3

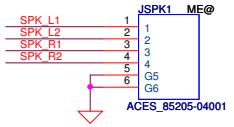




2009/11/02 Modify

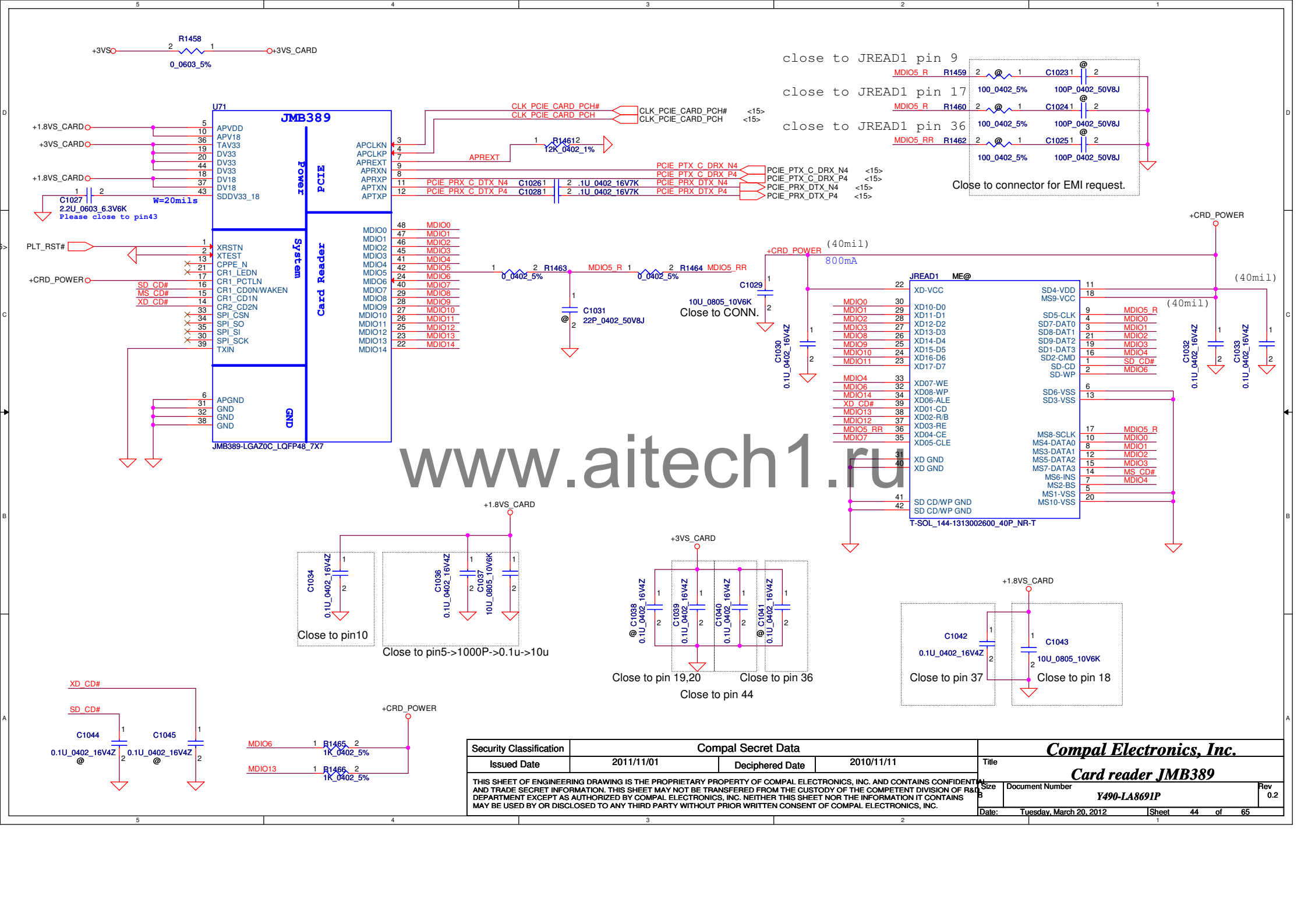
Reserve for ESD request.

Speaker Conn.



Security Classification	Compal Secret Data		
Issued Date	2011/11/01	Deciphered Date	2012/03/09

Compal Electronics, Inc.			
Title	AMP-MAX98400BETG+T		
Size: Custom	Document Number: Y490-LA8691P		Rev: 0.2
Date: Tuesday, March 20, 2012	Sheet 43 of 65		



Security Classification	Compal Secret Data		
Issued Date	2011/11/01	Deciphered Date	2010/11/11

Compal Electronics, Inc.

Title: **Card reader JMB389**

Size	Document Number	Rev
B	Y490-LA8691P	0.2

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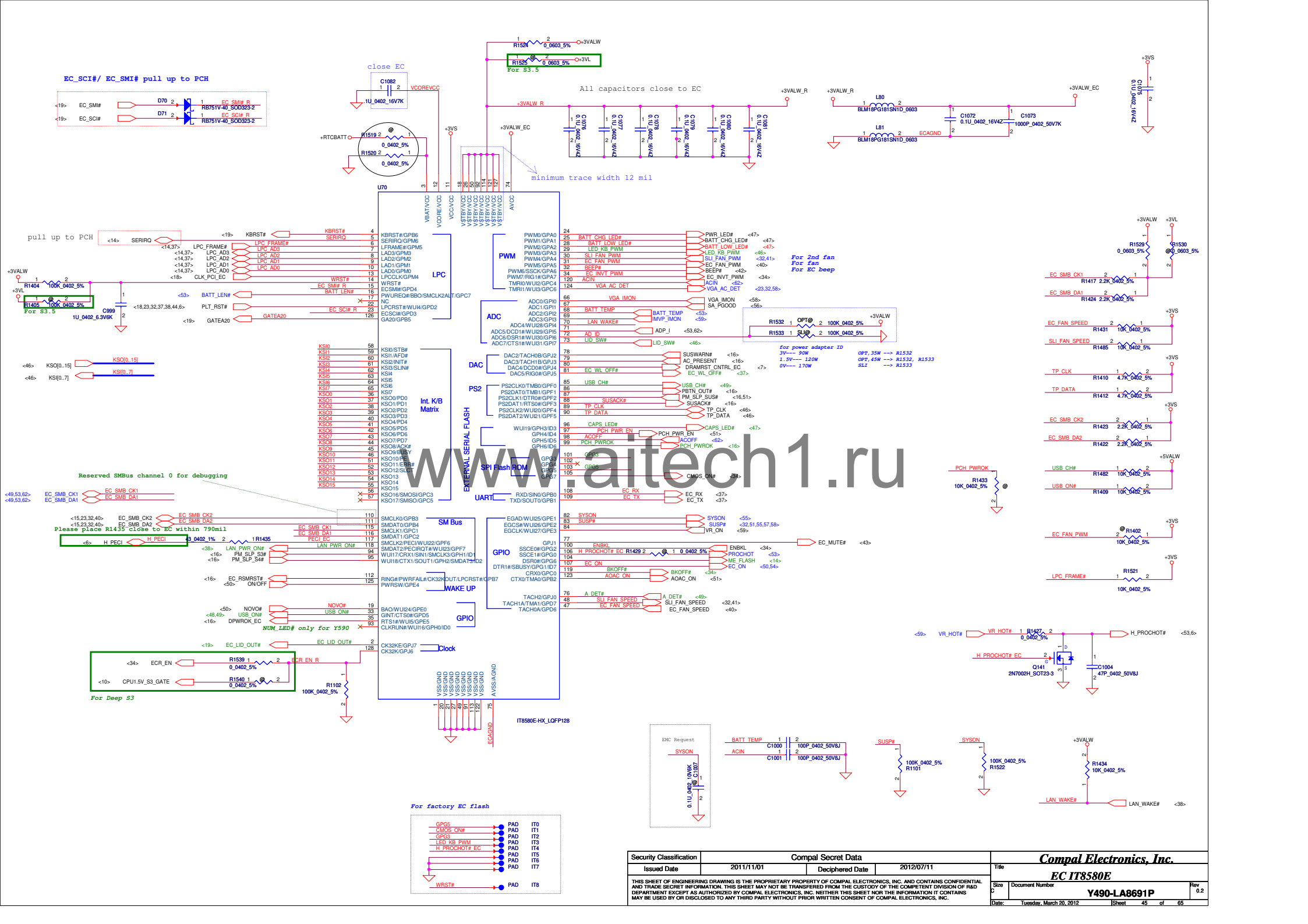
EC_SCI#/ EC_SMI# pull up to PCH
close EC
All capacitors close to EC
minimum trace width 12 mil
U70
IT8580E-HX_LQFP128
LPC
PWM
ADC
DAC
PS2
Int. K/B Matrix
EXTERNAL SERIAL FLASH
SPI Flash ROM
UART
SM Bus
GPIO
WAKE UP
Clock
pull up to PCH
For S3.5
For 2nd fan
For fan
For EC beep
for power adapter ID
3V--- 90W
1.5V--- 120W
0V--- 170W
Reserved SMBus channel 0 for debugging
Please place R1435 close to EC within 790mil
NUM_LED# only for Y590
For Deep S3
For factory EC flash
EMC Request
www.aitech1.ru
Security Classification
Compal Secret Data
Issued Date
2011/11/01
Deciphered Date
2012/07/11
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Compal Electronics, Inc.
Title
EC IT8580E
Size
C
Document Number
Y490-LA8691P
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0.2
Date:
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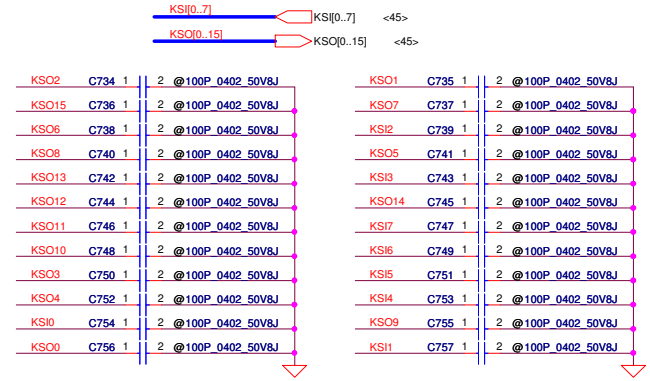
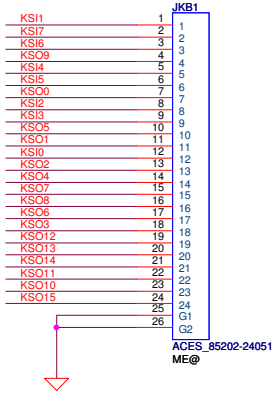
of
65

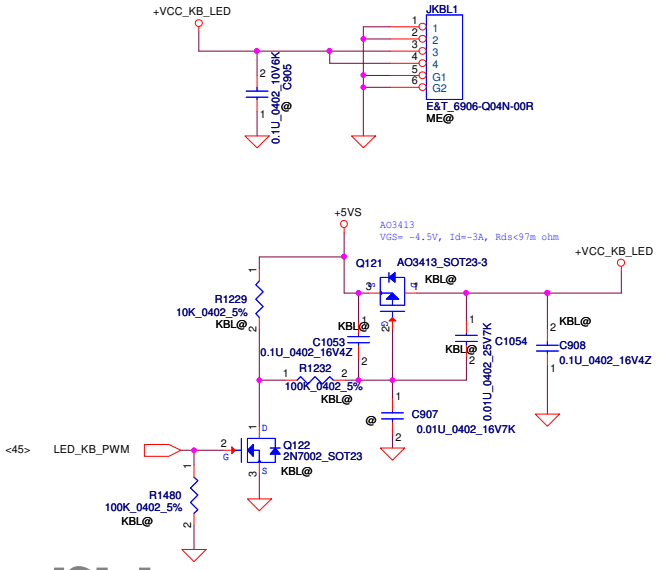
14" INT_KBD Conn.



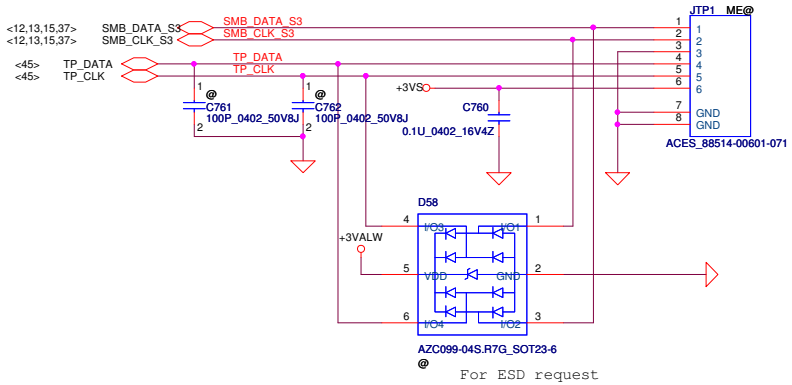
CONN PIN define need double check



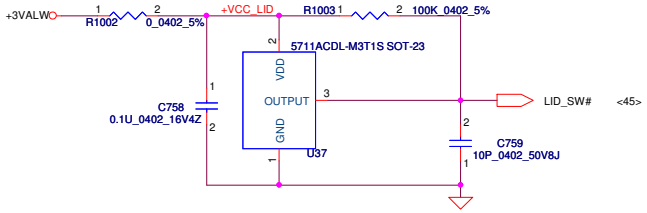
KB Lighting CONN.4pin



To TP/B Conn.

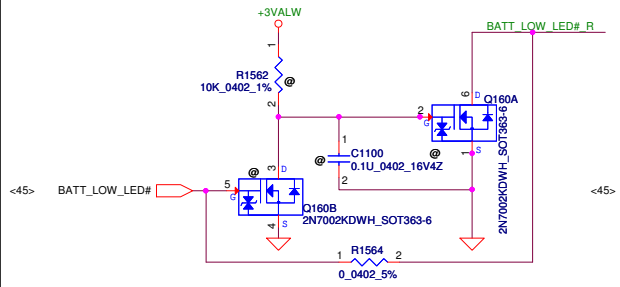


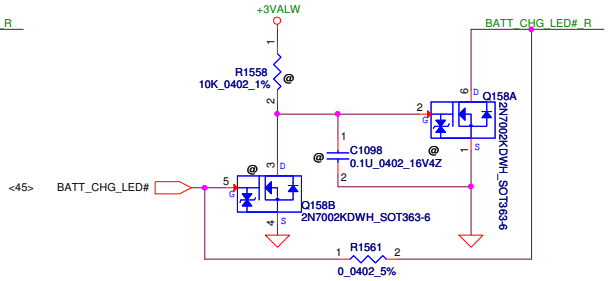
Lid Switch



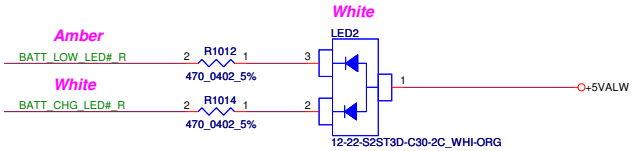
Security Classification	Compal Secret Data		
Issued Date	2011/11/01	Deciphered Date	2012/12/31

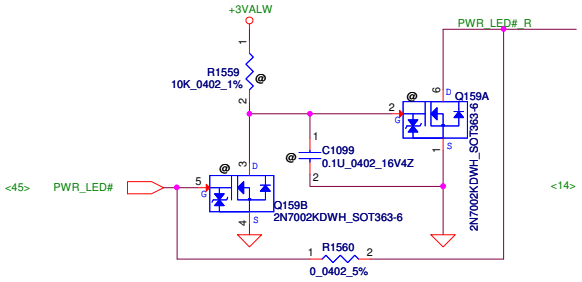
Compal Electronics, Inc.			
Title: KB /SW /LPC Debug Conn.			
Size: Custom	Document Number: Y490-LA8691P		Rev: 0.2
Date: Tuesday, March 20, 2012	Sheet 46 of 65		

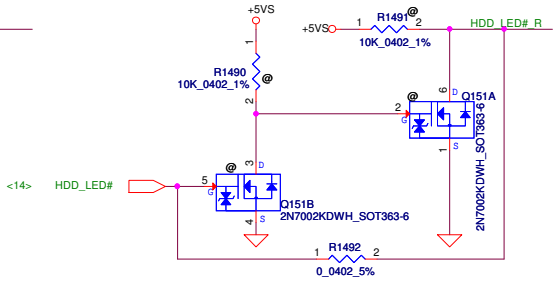




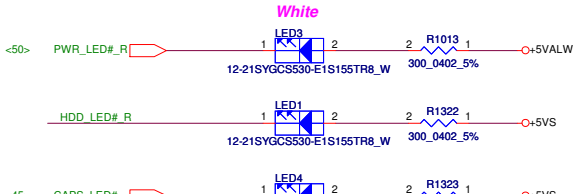
BATT CHARGE/LOW LED

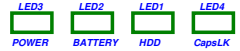




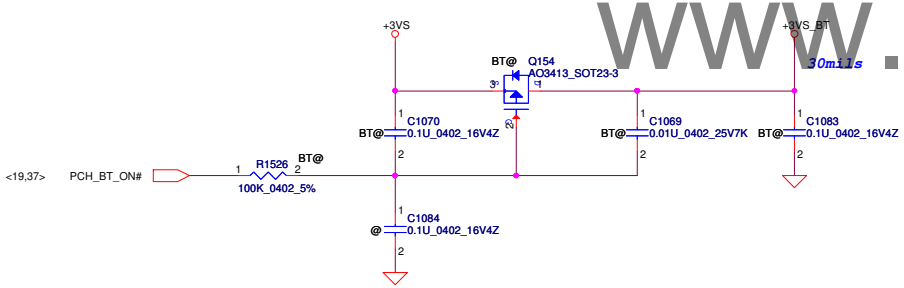


PWR LED HDD LED CapsLK LED

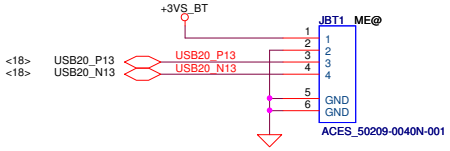




BlueTooth DC



BT Conn.



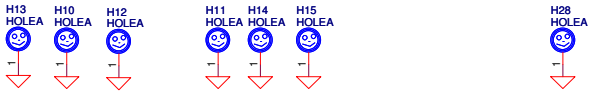
Screw Hole

CPU and GPU: H_3P8X 6

C: H_3P8X 3 B: H_3P8X 3

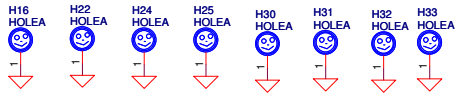
MIN PCIE: H_3P3 X 1

E: H_3P3X 1

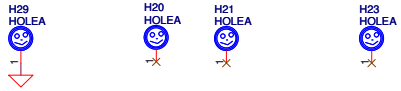


ME: H_8P0 X 8; H_3P3X 1; H_4P0X3P0N X 2; H_2P0X 1

A: H_2P8X 8



E: H_3P3X 1 H_4P0X3P0NX 3 H_2P0X 2



PCB Fedical Mark PAD

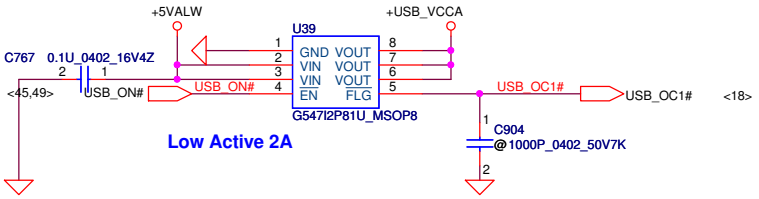
Security Classification	Compal Secret Data		
Issued Date	2011/11/01	Deciphered Date	2012/12/31

Compal Electronics, Inc.

Title: LED/EC SPI ROM/BT

Size: Custom	Document Number: Y490-LA8691P	Rev: 0.2
Date: Tuesday, March 20, 2012	Sheet 47 of 65	

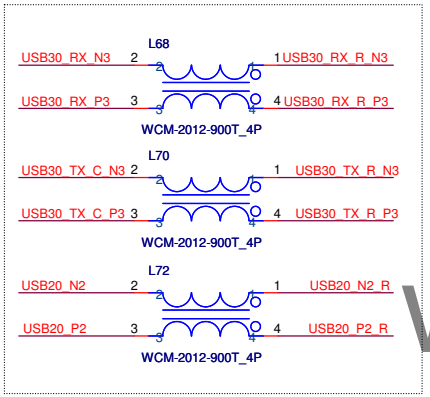
LEFT SIDE USB3.0 PORT X1

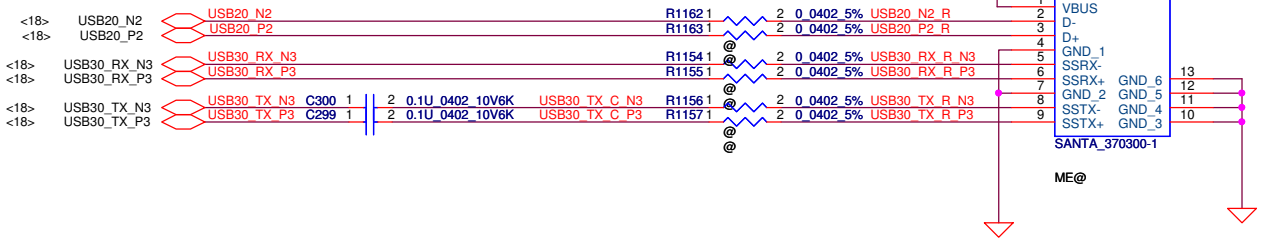


For EMI request

USB2.0 choke --> SM070000I00

USB3.0 Choke --> SM070001U00





For ESD request

Security Classification	Compal Secret Data For EMI request		Compal Electronics, Inc.
Issued Date	2011/11/01	Deciphered Date	2012/12/31
Title: USB3.0 ports			
Size: Custom	Document Number: Y490-LA8691P		Rev: 0.2
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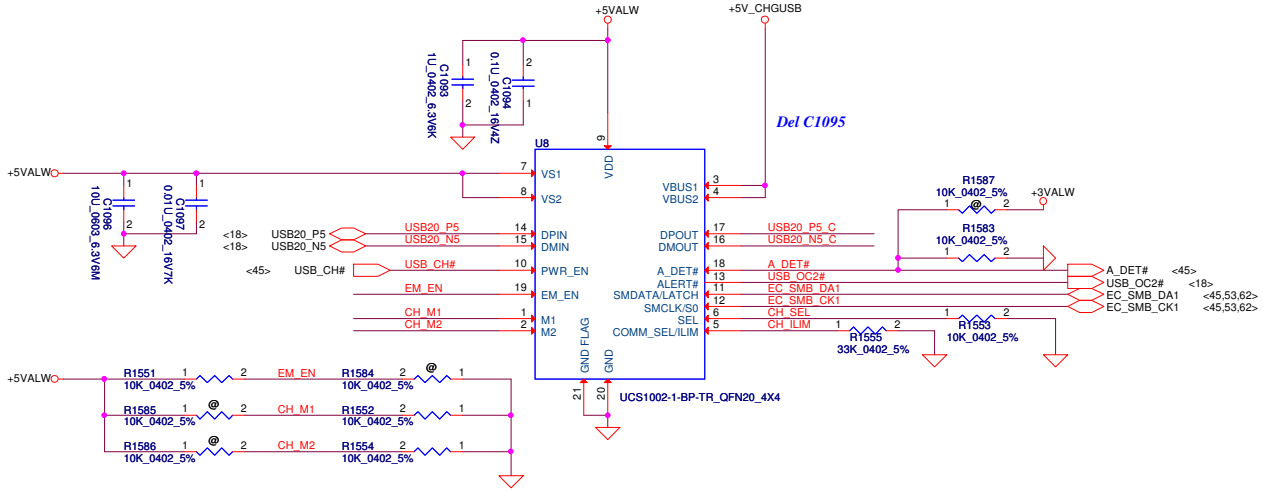
Sleep & Charge
Right side USB Charger Port (USB_Port5, near JMIC1)



Del C1095

Active Mode Selection:

	M1	M2	EM_EN	ACTIVE MODE
*	0	0	1	Dedicated Charger Emulation Cycle
	0	1	0	Date Pass-through
	0	1	1	BC1.2 DCP
	1	0	0	BC1.2 SDP
	1	0	1	Dedicated Charger Emulation Cycle
	1	1	0	Date Pass-through
	1	1	1	BC1.2 CDP

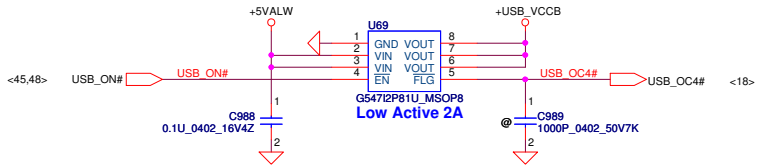
ILIM SETTING

	Pull Low
	0R-500mA
	10K-900mA
	12K-1000mA
	15K-1200mA
	18K-1500mA
	22K-1800mA
	27K-2000mA
*	33K-2500mA

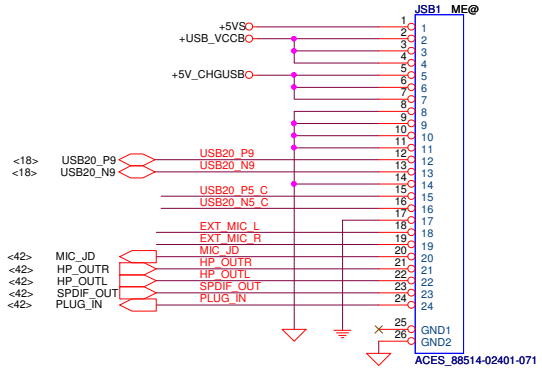
SEL Pin Decode

	Pull Low
	0R -1010_000
*	10K-1010_000
	12K-1010_000
	15K-1010_000
	18K-0110_000
	22K-0110_000
	27K-0110_000
	33K-0110_000

USB Power (USB20_P9)

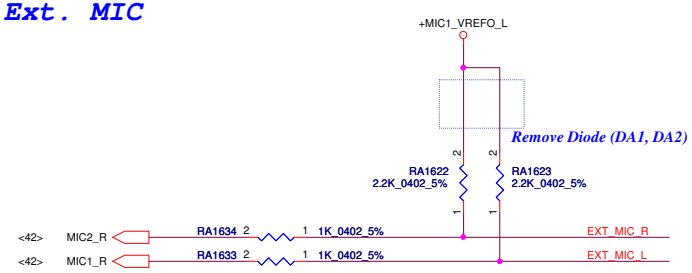


AUDIO/B Conn.



need change to 新貨 material
COMPAL : SP010015W1J
Footprint : 88514-0240N-071

Ext. MIC



Remove Diode (DA1, DA2)

Security Classification	Compal Secret Data		
Issued Date	2011/11/01	Deciphered Date	2012/12/31

Compal Electronics, Inc.

Title: Audio B Conn/USB charger

Size: Custom | Document Number: Y490-LA8691P | Rev: 0.2

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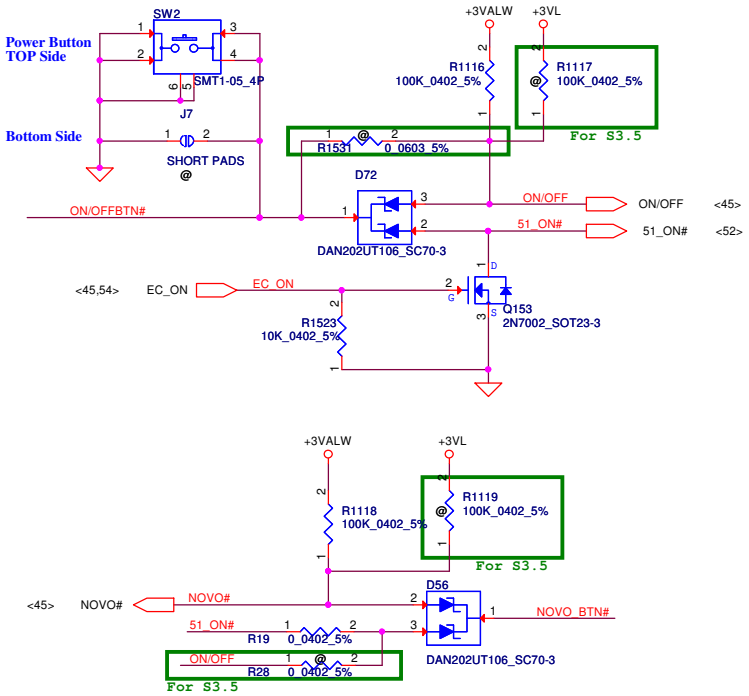
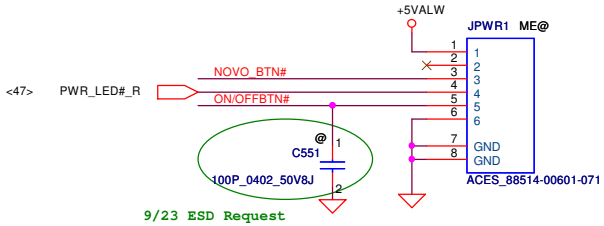
ON/OFF switch



Power Button/B link to Function/B Conn. 10pin



EMI REQUEST 1ST = SCA00000E00
2ST = SCA00000R00

Security Classification	Compal Secret Data		
Issued Date	2011/11/01	Deciphered Date	2012/12/31

Compal Electronics,Ltd.

Title: **other IO connector**

Size	Document Number	Rev
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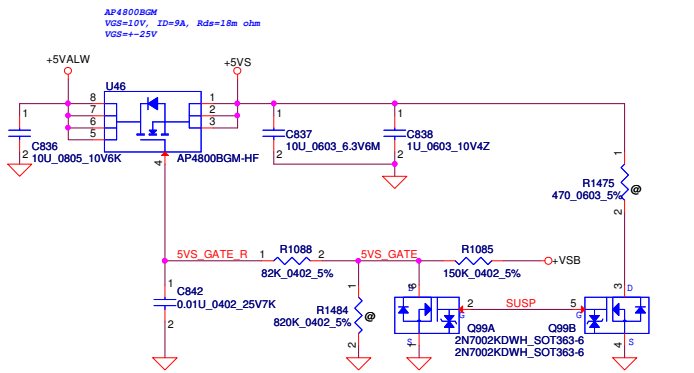
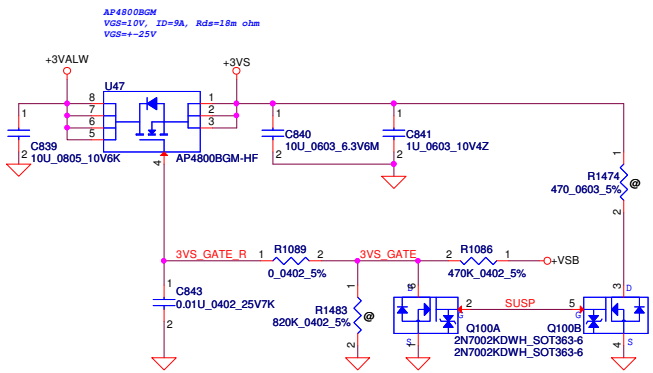
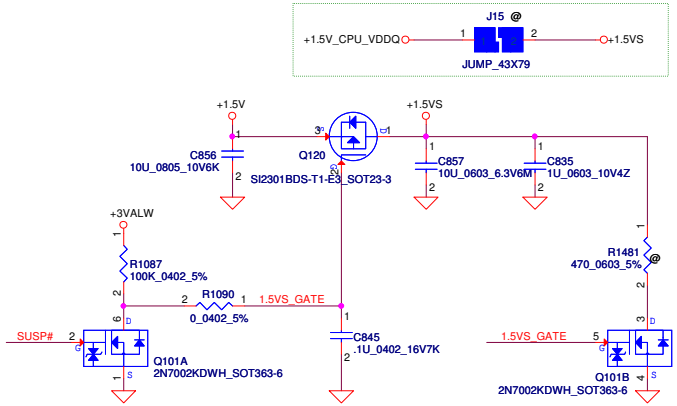
+5VALW to +5VS

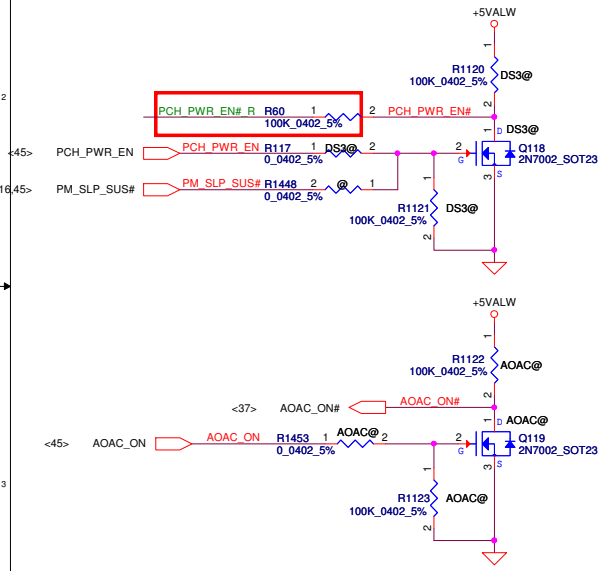


+3VALW to +3VS

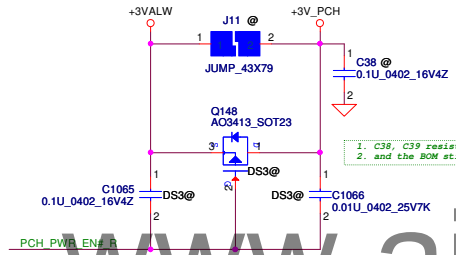


+1.5V to +1.5VS

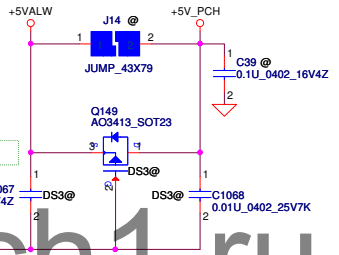


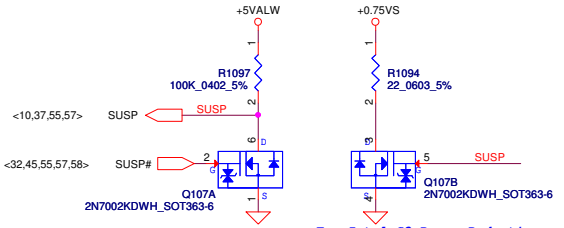


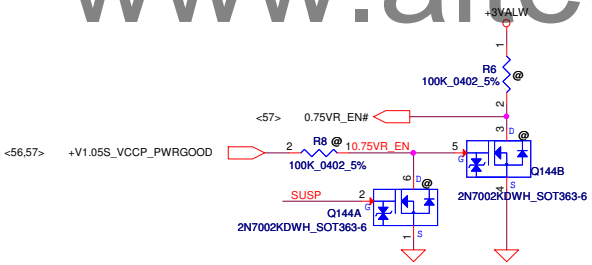
+3VALW to +3V_PCH



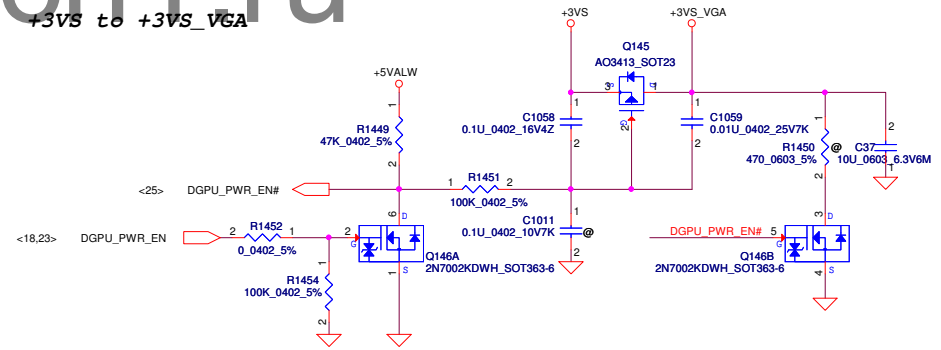
+5VALW to +5V_PCH



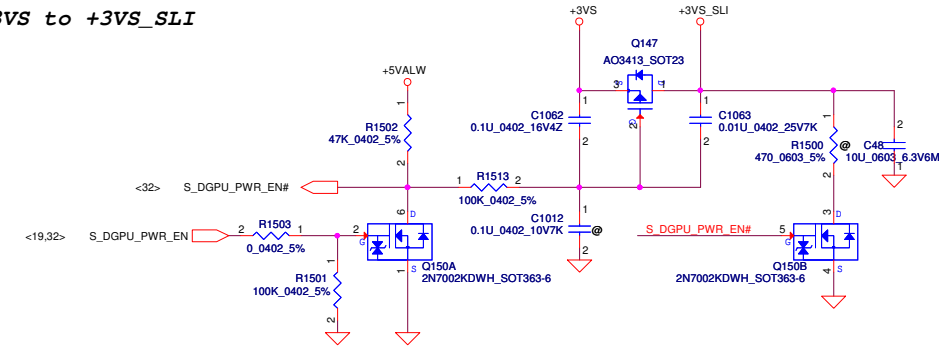




+3VS to +3VS_VGA



+3VS to +3VS_SLI



Security Classification	Compal Secret Data		
Issued Date	2011/11/01	Deciphered Date	2012/12/31

Compal Electronics, Inc.

Title: **DC Interface**

Size	Document Number	Rev
Custom	Y490-LA8691P	0.2

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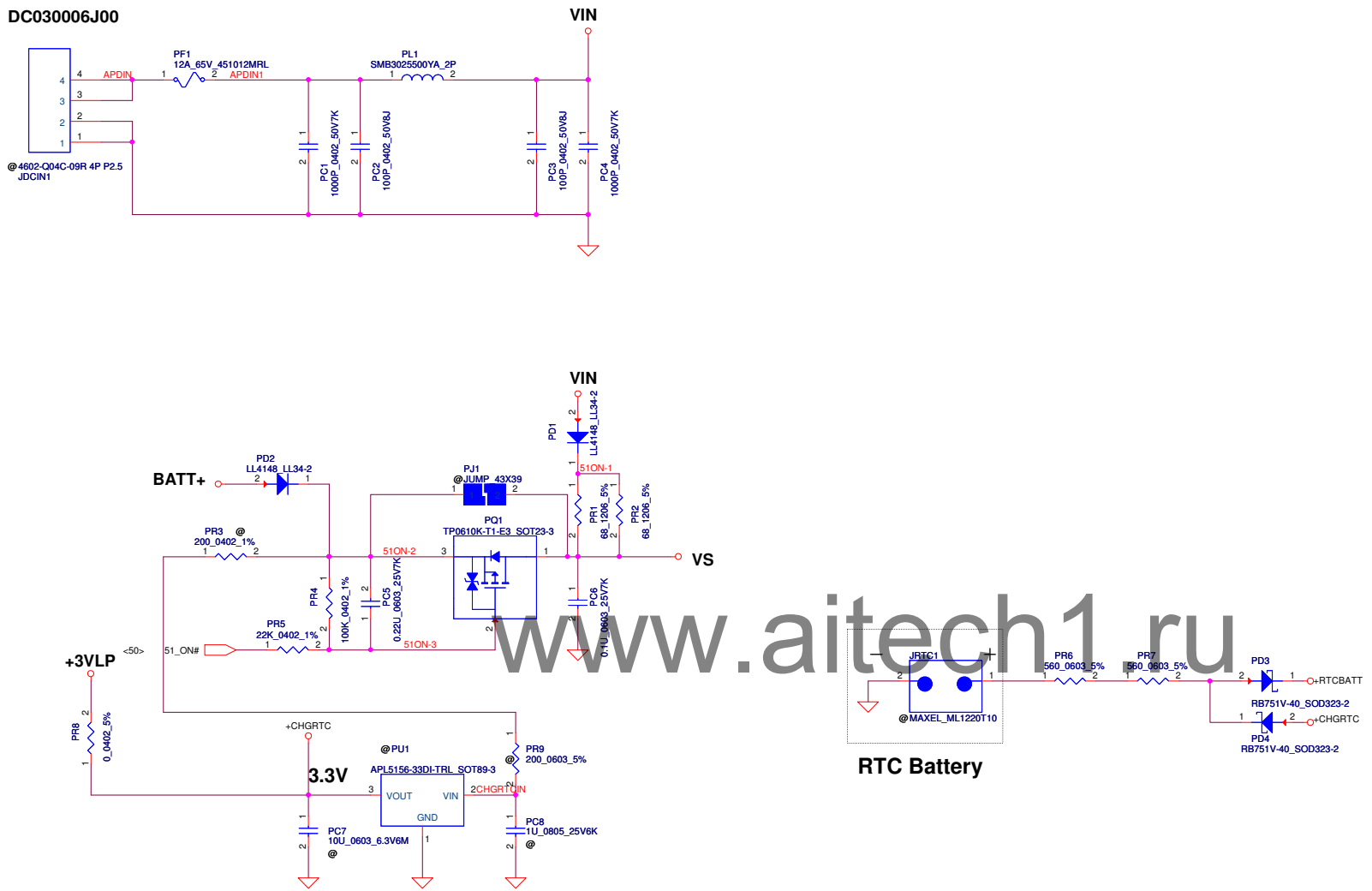

Security Classification	Compal Secret Data		
Issued Date	2011/06/30	Deciphered Date	2012/12/31

Compal Electronics, Inc.

Title: Vin Detector

Size: Custom | Document Number: Y490-LA8691P | Rev: 0.1

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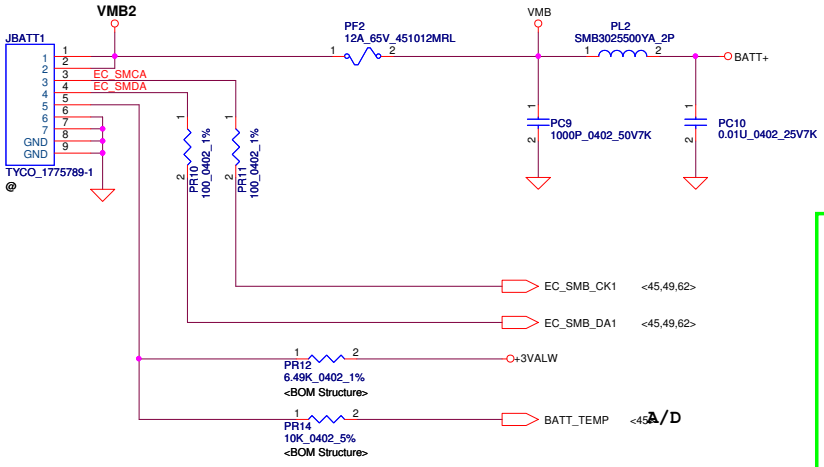
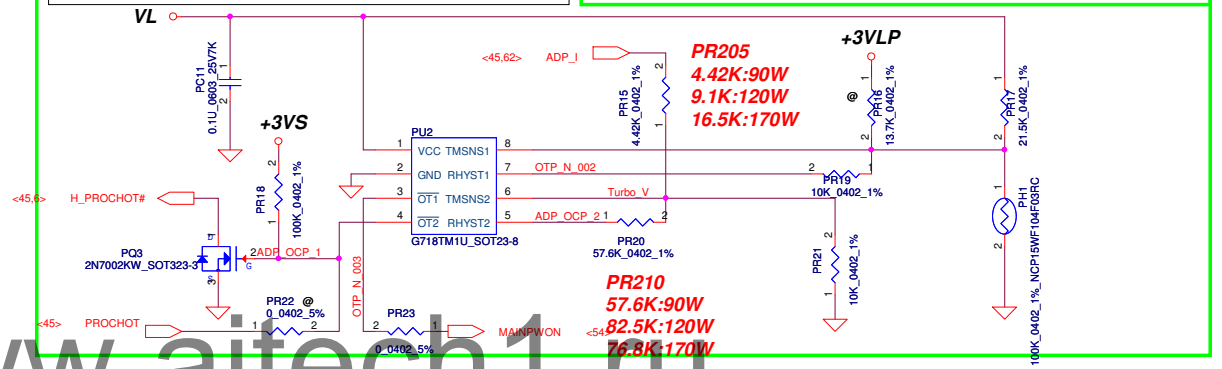
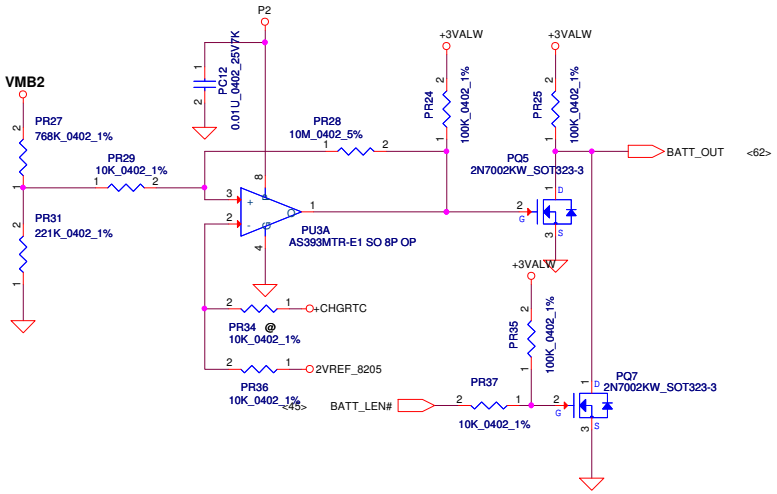
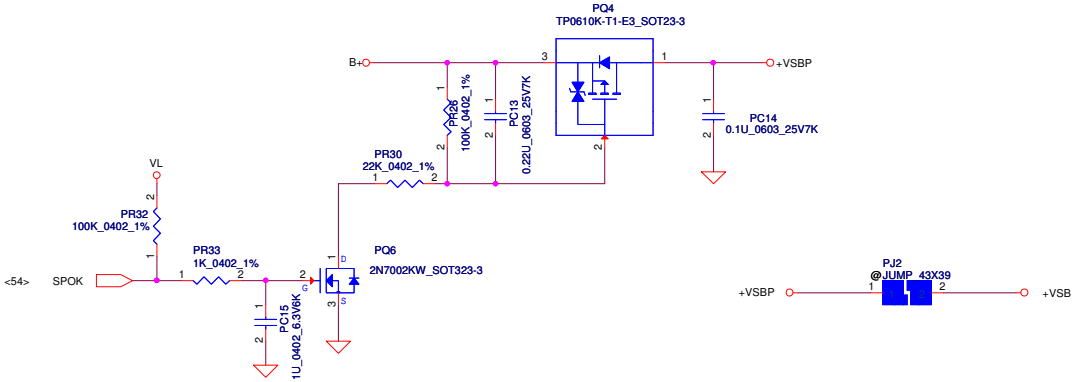


PH1 under CPU botten side :
CPU thermal protection at 92+-3 degree C
Recovery at 56 +-3 degree C

For KB930 --> Keep PU1 circuit
(Vth = 0.825V)
For KB9012 (Red square) --> Remove PU1 circuit, but keep PR206
PH201, PR205,PR211,PQ201,PR208,PR212



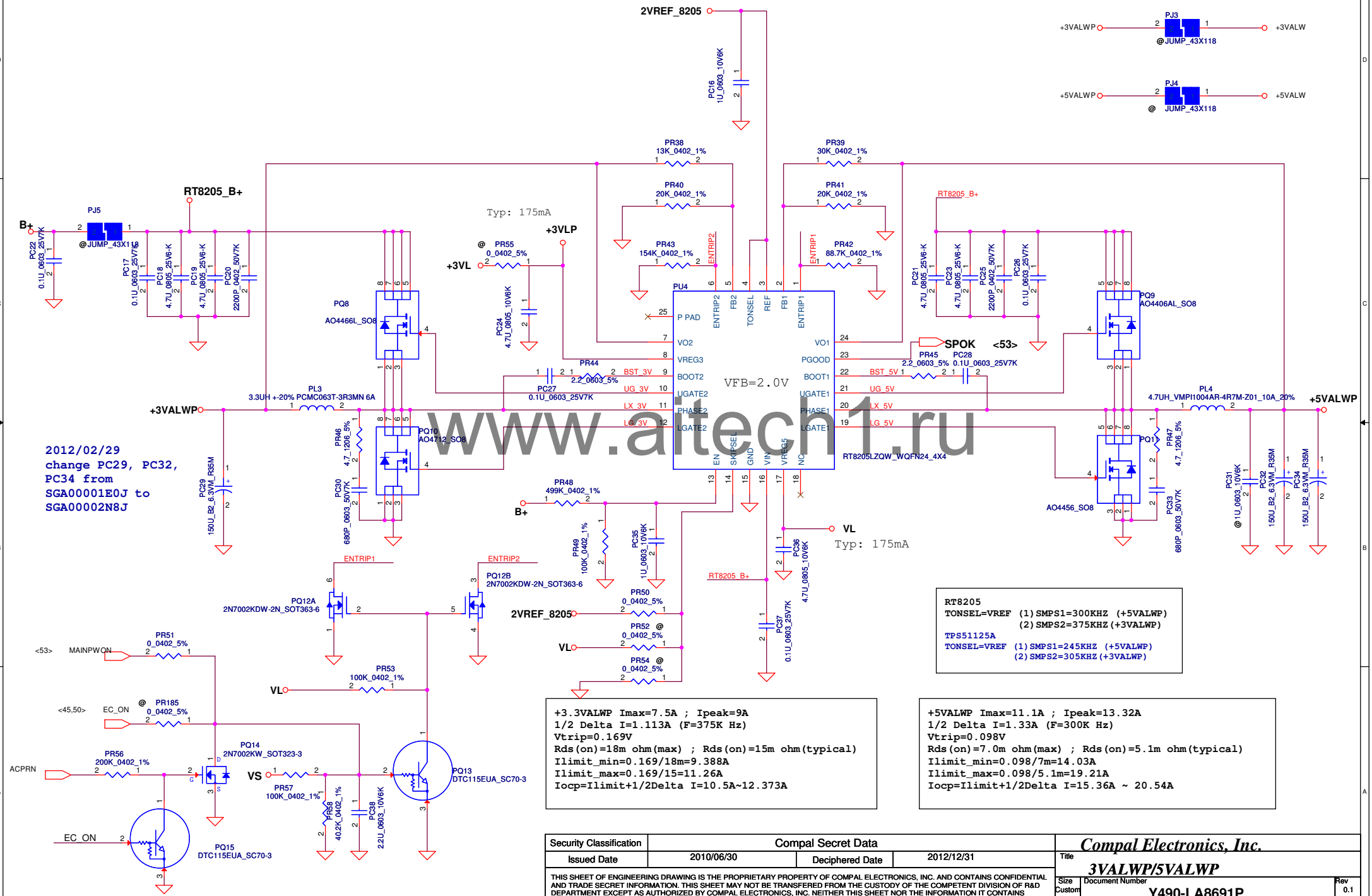




Security Classification	Compal Secret Data		
Issued Date	2010/06/30	Deciphered Date	2012/12/31

Compal Electronics, Inc.			
Title: BATTERY CONN/OTP			
Size: Custom	Document Number: Y490-LA8691P		Rev: 0.1
Date: Tuesday, March 20, 2012	Sheet 53 of 65		

Note:
Use TPS51125 IC can remove RTC refernece LDO
Use TPS51427 IC must keep RTC refernece LDO



RT8205
TONSEL=VREF (1)SMPS1=300KHZ (+5VALWP)
(2)SMPS2=375KHZ(+3VALWP)
TPS51125A
TONSEL=VREF (1)SMPS1=245KHZ (+5VALWP)
(2)SMPS2=305KHZ(+3VALWP)

+3.3VALWP Imax=7.5A ; Ipeak=9A
1/2 Delta I=1.113A (F=375K Hz)
Vtrip=0.169V
Rds(on)=18m ohm(max) ; Rds(on)=15m ohm(typical)
Ilimit_min=0.169/18m=9.388A
Ilimit_max=0.169/15=11.26A
Iocp=Ilimit+1/2Delta I=10.5A~12.373A

+5VALWP Imax=11.1A ; Ipeak=13.32A
1/2 Delta I=1.33A (F=300K Hz)
Vtrip=0.098V
Rds(on)=7.0m ohm(max) ; Rds(on)=5.1m ohm(typical)
Ilimit_min=0.098/7m=14.03A
Ilimit_max=0.098/5.1m=19.21A
Iocp=Ilimit+1/2Delta I=15.36A ~ 20.54A

Security Classification	Compal Secret Data		
Issued Date	2010/06/30	Deciphered Date	2012/12/31

Compal Electronics, Inc.

Title: 3VALWP/5VALWP

Size	Document Number	Rev
Custom	Y490-LA8691P	0.1

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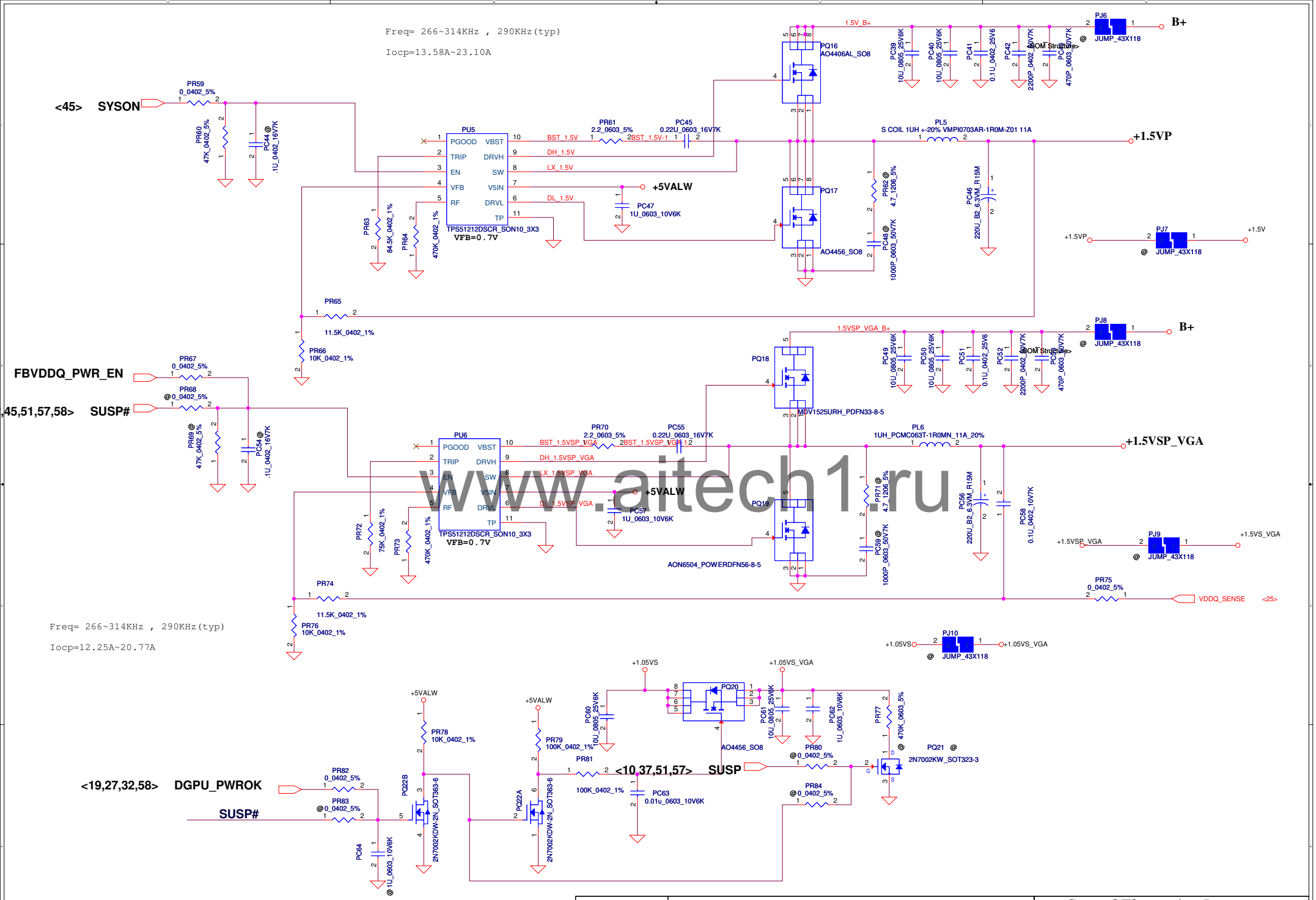


Security Classification	Compal Secret Data		
Issued Date	2010/06/30	Deciphered Date	2012/12/31

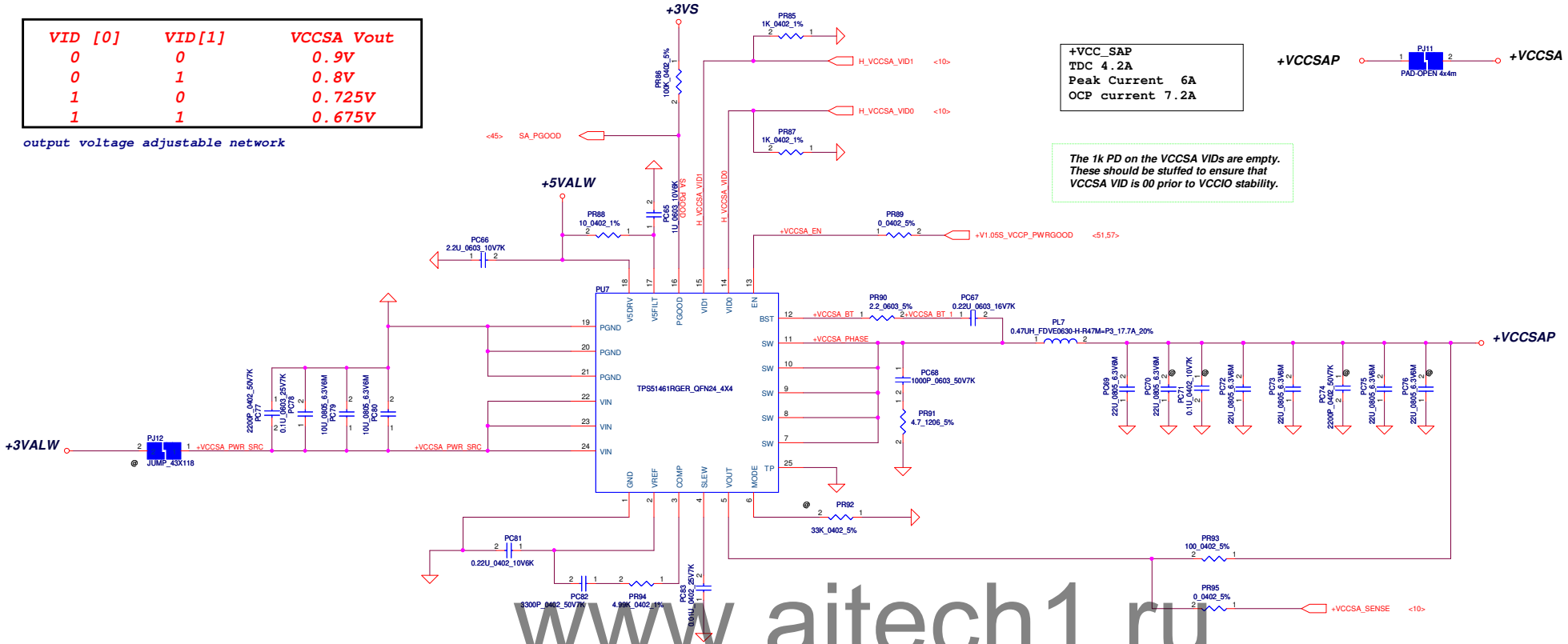
Compal Electronics, Inc.			
Title	1.5VP/1.5VSP_VGA/1.05VSP_VGA		
Size: Custom	Document Number: Y490-LA8691P		Rev: 0.2
Date: Tuesday, March 20, 2012	Sheet 55 of 65		

VID [0]	VID[1]	VCCSA Vout
0	0	0.9V
0	1	0.8V
1	0	0.725V
1	1	0.675V

output voltage adjustable network

+VCC_SAP
TDC 4.2A
Peak Current 6A
OCP current 7.2A

The 1k PD on the VCCSA VIDs are empty. These should be stuffed to ensure that VCCSA VID is 00 prior to VCCIO stability.



Security Classification	Compal Secret Data		
Issued Date	2011/06/30	Deciphered Date	2012/12/31

Compal Electronics, Inc.

Title: VCCSAP/1.05S_VCCPP

Size	Document Number	Rev
C	Y490-LA8691P	0.1

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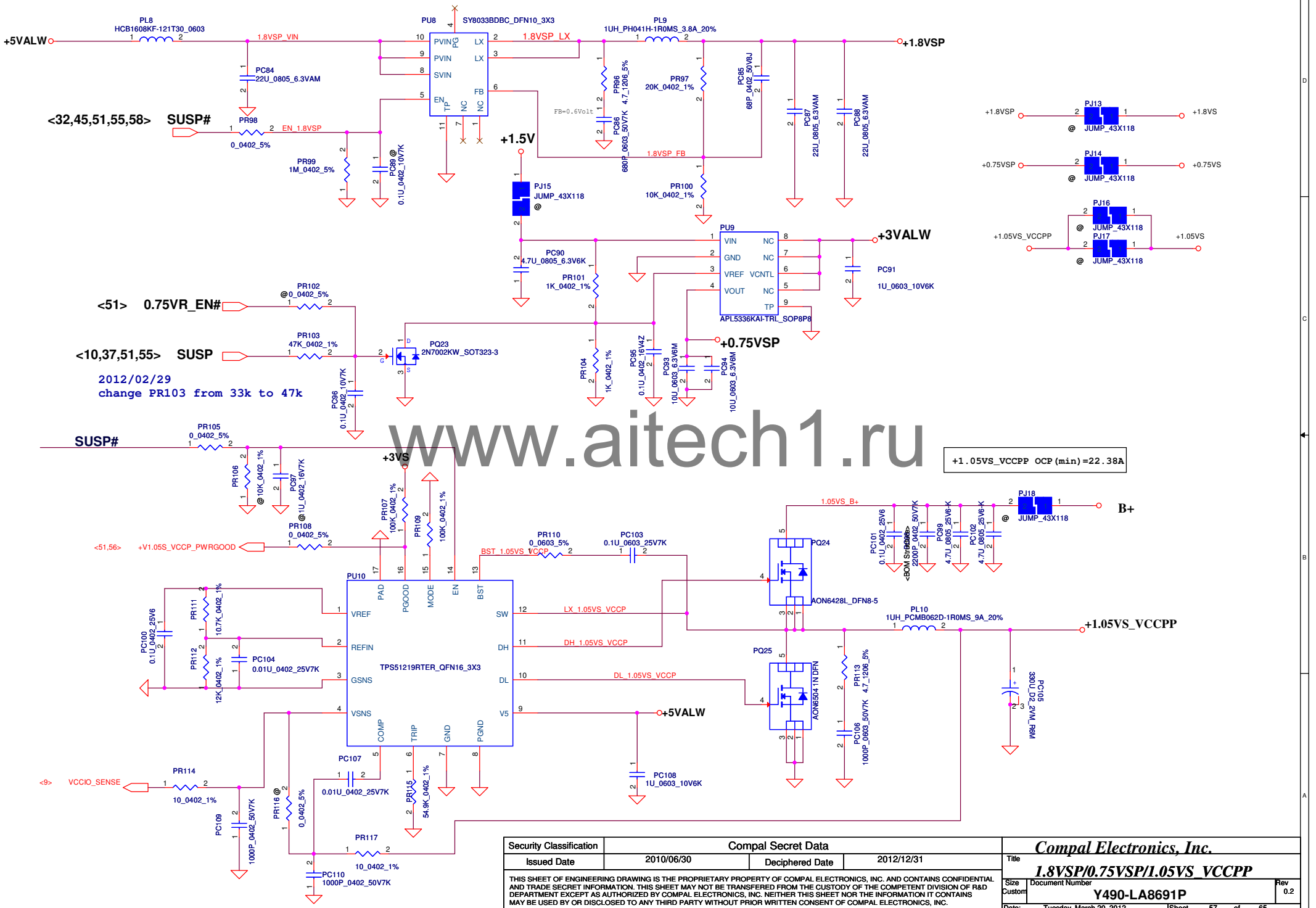


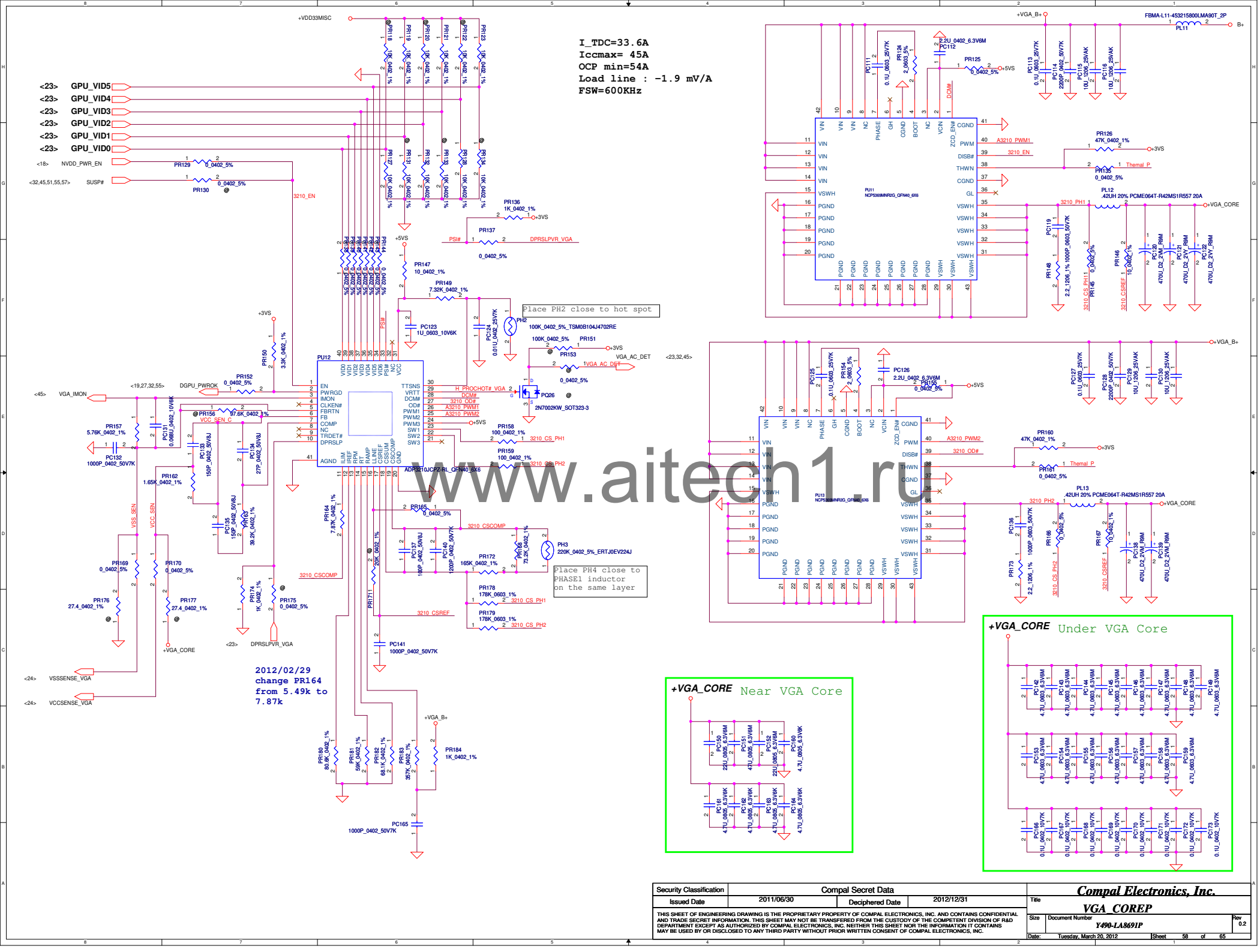
Security Classification	Compal Secret Data		
Issued Date	2010/06/30	Deciphered Date	2012/12/31

Compal Electronics, Inc.

Title: 1.8VSP/0.75VSP/1.05VS_VCCPP

Size	Document Number	Rev
Custom	Y490-LA8691P	0.2

Date: Tuesday, March 20, 2012 Sheet 57 of 65



Security Classification	Compal Secret Data		
Issued Date	2011/06/30	Deciphered Date	2012/12/31

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Compal Electronics, Inc.

Title: **VGA_COREP**

Size	Document Number	Rev
	Y490-LA8691P	0.2

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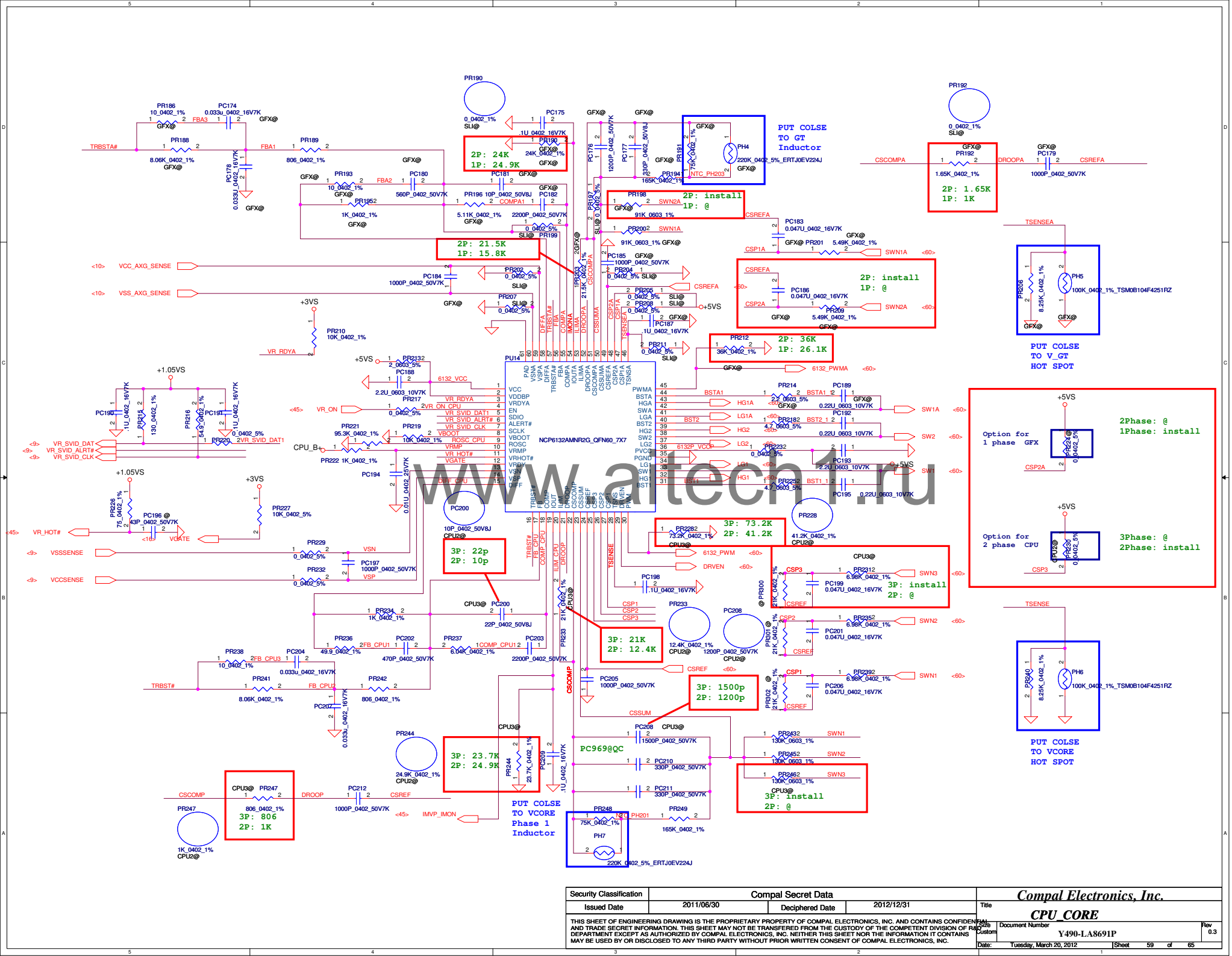

Security Classification	Compal Secret Data		
Issued Date	2011/06/30	Deciphered Date	2012/12/31

Compal Electronics, Inc.

Title: CPU_CORE

Size	Document Number	Rev
Custom	Y490-LA8691P	0.3

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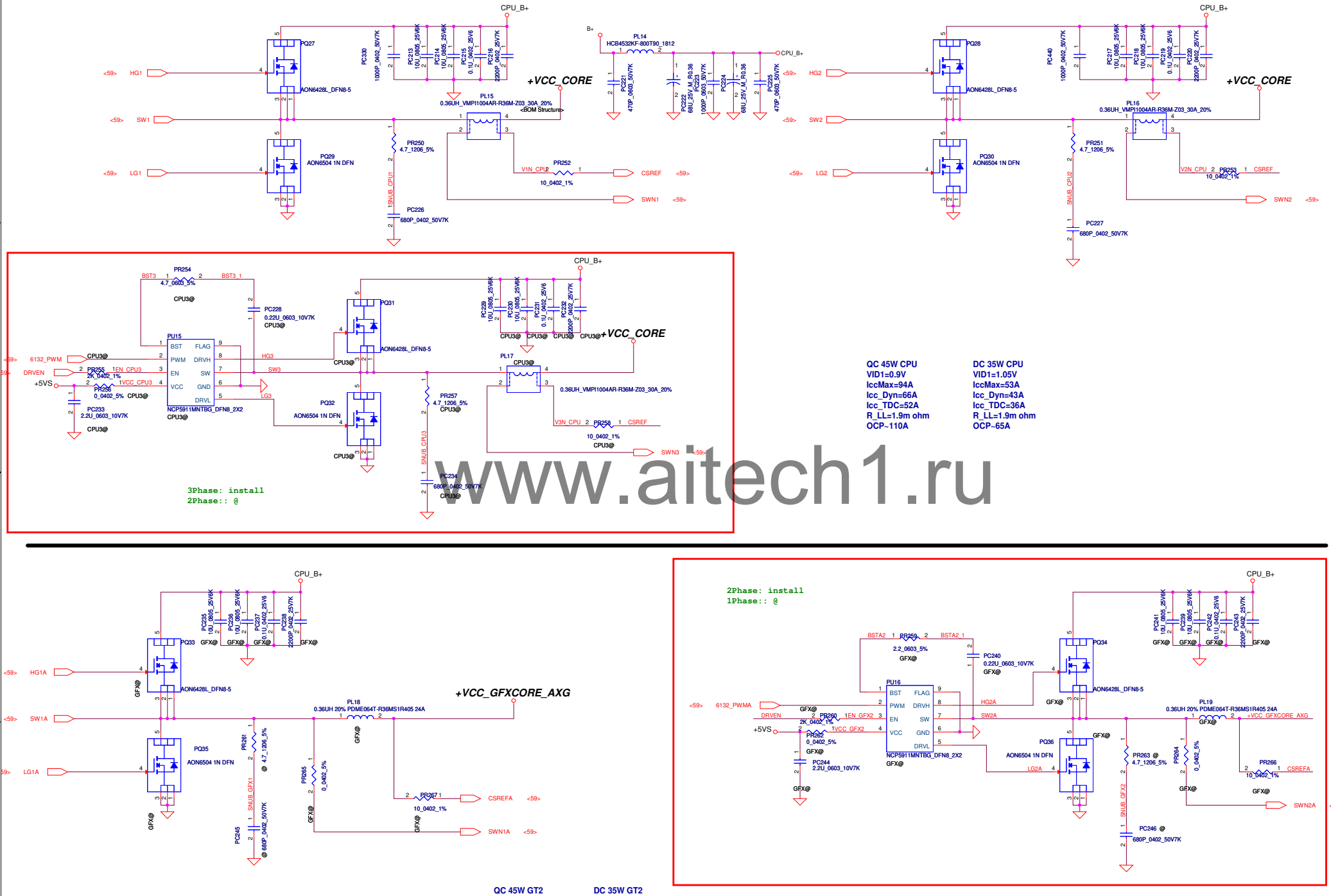

Security Classification	Compal Secret Data		
Issued Date	2011/06/30	Deciphered Date	2012/12/31

Compal Electronics, Inc.			
Title: CPU_CORE			
Size: C	Document Number: Y490-LA8691P		Rev: 0.3
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+CPU_CORE

+VCC_CORE

PC247 10U_0805_6.3VAM
PC248 10U_0805_6.3VAM
PC249 10U_0805_6.3VAM
PC250 10U_0805_6.3VAM
PC251 10U_0805_6.3VAM
PC252 10U_0805_6.3VAM
PC253 10U_0805_6.3VAM
PC254 10U_0805_6.3VAM
PC255 10U_0805_6.3VAM
PC256 10U_0805_6.3VAM
PC257 10U_0805_6.3VAM

+VCC_CORE

PC266 22U_0805_6.3V6M
PC267 22U_0805_6.3V6M
PC268 22U_0805_6.3V6M
PC269 22U_0805_6.3V6M
PC270 22U_0805_6.3V6M
PC290 22U_0805_6.3V6M
PC291 22U_0805_6.3V6M
PC292 22U_0805_6.3V6M
PC293 22U_0805_6.3V6M
PC294 22U_0805_6.3V6M
PC306 22U_0805_6.3V6M
PC307 22U_0805_6.3V6M
PC308 22U_0805_6.3V6M
PC309 22U_0805_6.3V6M
PC310 22U_0805_6.3V6M
PC313 22U_0805_6.3V6M
PC314 22U_0805_6.3V6M
PC315 22U_0805_6.3V6M
PC316 22U_0805_6.3V6M

PC8,PC21,PC22,PC63

+VCC_CORE

PC317 470U_D2_2VM_R4.5M
PC318 470U_D2_2VM_R4.5M
PC319 470U_D2_2VM_R4.5M
PC320 470U_D2_2VM_R4.5M
PC321 470U_D2_2VM_R4.5M
PC322 470U_D2_2VM_R4.5M

DC:PC73,PC74,PC75,PC76,PC77,PC78(330uF/9m)
QC:PC76,PC78(470uF/4.5m),PC73,PC74,PC75(330uF/9m)

+VCC_GFXCORE_AXG

+VCC_GFXCORE_AXG

PC258 22U_0805_6.3V6M GFX@
PC259 22U_0805_6.3V6M GFX@
PC260 22U_0805_6.3V6M GFX@
PC261 22U_0805_6.3V6M GFX@
PC262 22U_0805_6.3V6M GFX@
PC263 22U_0805_6.3V6M GFX@
PC264 22U_0805_6.3V6M GFX@
PC265 22U_0805_6.3V6M GFX@
PC282 22U_0805_6.3V6M GFX@
PC283 22U_0805_6.3V6M GFX@
PC284 22U_0805_6.3V6M GFX@
PC285 22U_0805_6.3V6M GFX@
PC286 22U_0805_6.3V6M GFX@
PC287 22U_0805_6.3V6M GFX@
PC288 22U_0805_6.3V6M GFX@
PC289 22U_0805_6.3V6M GFX@
PC303 330U_D2_2VM_R9M GFX@
PC304 330U_D2_2VM_R9M GFX@
PC305 330U_D2_2VM_R9M GFX@

PC59@DC

PC38,PC39,PC40,PC41

PC38,PC39,PC40,PC41

Below is 458544_CRV_PDDG_0.5 Table 5-8.

Socket Bottom	5 x 22 µF (0805) 5 x (0805) no-stuff sites
Socket Top	7 x 22 µF (0805) 2 x (0805) no-stuff sites

+1.05VS

PC271 22U_0805_6.3V6M
PC272 22U_0805_6.3V6M
PC273 22U_0805_6.3V6M
PC274 22U_0805_6.3V6M
PC275 22U_0805_6.3V6M
PC276 22U_0805_6.3V6M
PC277 22U_0805_6.3V6M
PC278 22U_0805_6.3V6M
PC279 22U_0805_6.3V6M
PC280 22U_0805_6.3V6M
PC281 22U_0805_6.3V6M
PC295 22U_0805_6.3V6M
PC296 22U_0805_6.3V6M
PC297 22U_0805_6.3V6M
PC298 22U_0805_6.3V6M
PC299 22U_0805_6.3V6M
PC300 22U_0805_6.3V6M
PC301 22U_0805_6.3V6M
PC302 22U_0805_6.3V6M
PC311 330U_D2_2VM_R6M
PC312 330U_D2_2VM_R6M

PC32,PC49,PC54,PC55,PC56

Security Classification	Compal Secret Data		
Issued Date	2011/06/30	Deciphered Date	2012/12/31

Compal Electronics, Inc.

Title: CPU_CORE1

Size | Document Number: Y490-LA8691P | Rev: 0.1

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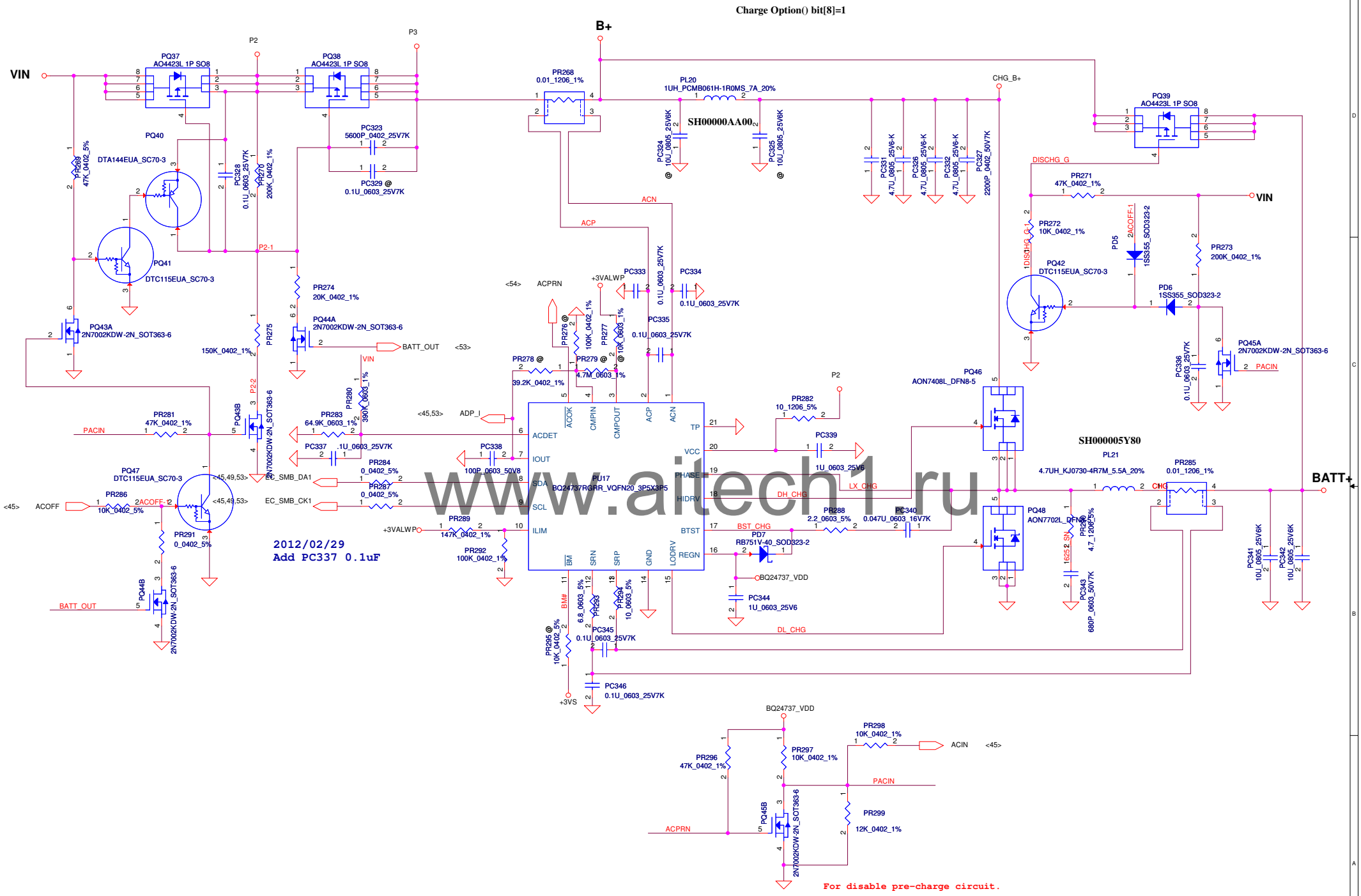
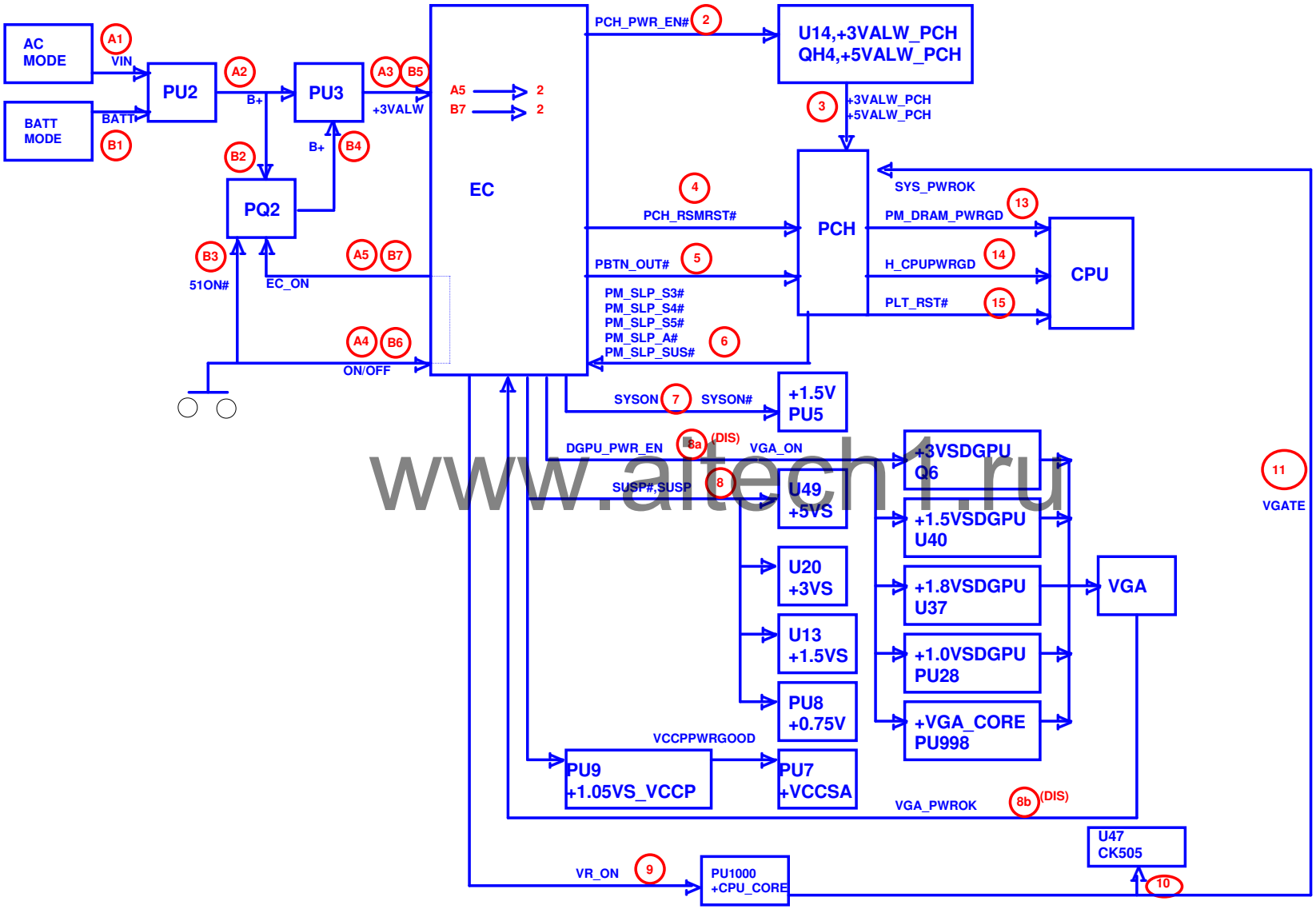


Security Classification	Compal Secret Data		
Issued Date	2010/06/30	Deciphered Date	2012/12/31

Compal Electronics, Inc.	
Title	CHARGER
Size	Document Number: Y490-LA8691P
Rev	0.2
Date: Tuesday, March 20, 2012	Sheet 62 of 65



Security Classification	Compal Secret Data		
Issued Date	2011/07/21	Deciphered Date	2012/12/31

Compal Electronics, Inc.

Title: Power sequence

Size: Custom | Document Number: LA-8691P | Rev: 0.1

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Version change list (P.I.R. List)

Item	Reason for change	PG#	Modify List	Date	Phase
1	Reserve 0.1uF for Charger IC	51	Reserve PC321	201109/27	B test
2	EMI Request		change PR322,PR407,PR408,PR503,PR511,PR606,PR804,PR827 to 2.2 ohm add PC526,PC527,PC970,PC971(470uF)	201109/27	B test
3	Combine 1.05V	51	Remove one power rail +V1.05S_VCCPP Pop PR722,PR712,PR718	201109/27	B test
4	Discharge for +1.05VS_VGA by NV Request	53	Reserve PR528	201109/27	B test
5	Set VGA_CORE VBOOT voltage	56	unpop PR806 change PR813 to 147K ohm	201109/27	B test
6	For VGA_CORE power saving by NV Request	56	add PR838 0ohm	201109/27	B test
7	for CPU_CORE load line adjust	57	add PC969	201109/27	B test
8	to prevent MOS over temperature	55/58	change PQ702,PQ901,PQ902,PQ905 TPCA8065	201109/27	B test
9	for CPU_CORE test	59	Reserve PC77,PC78	201109/27	B test
10					
11					
12					
13					
14					
15					
16					
17					

Security Classification	Compal Secret Data		
Issued Date	2011/06/30	Deciphered Date	2012/12/31

Compal Electronics, Inc.

Title: PIR (PWR)

Size: Custom | Document Number: Y490-LA8691P | Rev: 0.1

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HW PIR (Product Improve Record)

QIQY5 LA-8691P SCHEMATIC CHANGE LIST
REVISION CHANGE: 0.2
GERBER-OUT DATE: 2012/03/09

NO	DATE	PAGE	MODIFICATION LIST		PURPOSE
01)	03/14	10	R64	Change R64 BOM structure from "@" to "DS3@"	For Deep S3 Function

Security Classification	Compal Secret Data		
Issued Date	2011/07/21	Deciphered Date	2012/12/31

Compal Electronics, Inc.

Title: LA-6882P PIR (HW)

Size: Custom | Document Number | Rev: 0.1

Date: Tuesday, March 20, 2012 | Sheet 65 of 65